4-bit Johnson Counter with Ring Oscillator using SKY130nm PDK

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***Abstract*—In this paper, I am going to Design and Implement a 4-bit Johnson Counter with Ring Oscillator using Verilog HDL and SKY130nm PDK. Design will be implemented using Verilog Code using esim and Makerchip Software. Mixed Signal Circuits contain both analog and digital part of a circuit. In this design we have implemented Johnson counter using Verilog code and Ring oscillator using CMOS circuit. As this is a mixed signal circuit, we will have complete implementation from HDL code to schematic implementation and we can verify the output using Circuit Waveforms. This complete design and implementation is done using VLSI technology which has features such as high speed, low power, low cost, and small size.**

1. CIRCUIT DETAILS

A Johnson counter is also known as a k-bit switch-tail ring counter with 2k decoding gates which provides output for 2k timing signals. A k-bit ring counter circulates a single bit among the flip-flops and can provide k distinguishable states. To double the number of states the shift register must be connected as a switch-tail ring counter. In a switch-tail ring counter we connect the last flip flop to the input of first flip flop as shown in the reference diagrams. The register shifts its contents once to the right with every clock pulse, and at the same time, the complemented value of the E flip-flop is transferred into the A flip- flop. Here, the last inverter's output is connected to the first inverter's input through a feedback path. It performs operations in a ring type fashion hence known as Ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator. Time period of ring oscillator(T)=2*n*Td where Td=Propagation delay of each inverter, Frequency of ring oscillator(f)=1/T and n=Number of inverters. Figures 1 and 2 shown the Reference circuit diagram and figure 3 shown the reference circuit diagram.

2. REFERENCE CIRCUIT DIAGRAM

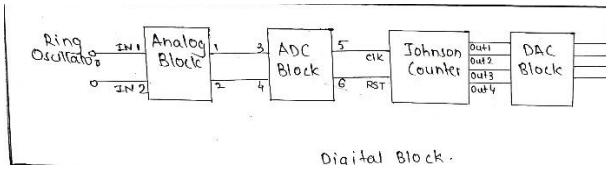

FIGURE 1

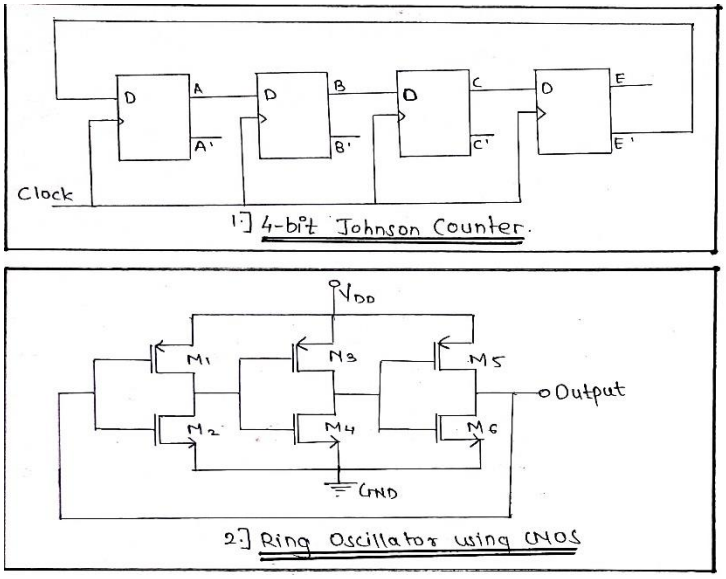

FIGURE 2

3. REFERENCE CIRCUIT WAVEFORM

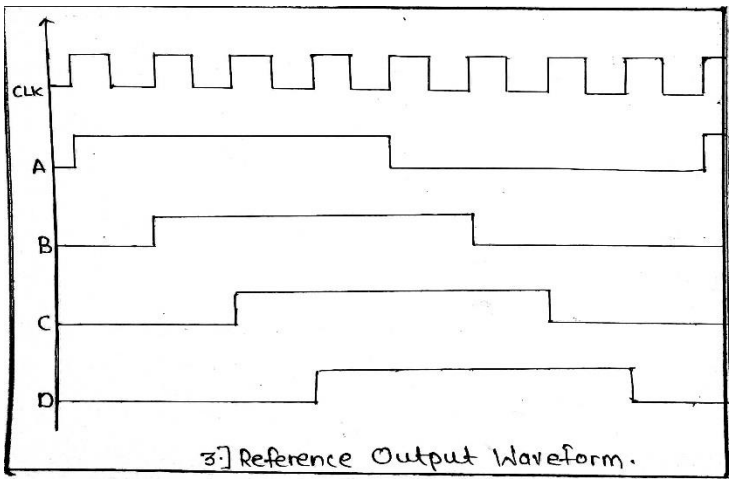

FIGURE 3

4. REFERENCES

[1] Stoev, I. I., Borodzhieva, A. N., & Mutkov, V. A. (2018). *FPGA Implementation of Johnson Counters Applied in the Educational Process. 2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME)*. doi:10.1109/siitme.2018.8599274

[2] V. Sikarwar, N. Yadav and S. Akashe, "Design and analysis of CMOS ring oscillator using 45 nm technology," 2013 3rd IEEE International Advance Computing Conference (IACC), Ghaziabad, 2013, pp. 1491- 149