Design of 2-Bit Magnitude Comparator In Mixed-Signal

Vishnu Bajjuri, Jyothishmathi Institute of Technology and Science

Abstract—A magnitude Comparator is a combinational circuit that compares two binary numbers in order to find out whether one binary number is equal, less than, or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and the other for B and have three output terminals, one for A > B condition, one for A = B condition, and one for A < B condition.

Index Terms—2 bit comparator, mixed-signal, MOS Transis- tors, Logic gates

I. Reference Circuit Details

Fig.1 shows the design of a 2-bit magnitude comparator in mixed-signal mode. In the diagram, a 2-bit magnitude comparator is split into two blocks: digital and analog. The digital portion of the circuit is implemented using Verilog. For the analog portion, the two 3-input "OR" gates and one 2-input "AND" gate are replaced with NMOS and PMOS transistors, making the circuit mixed-signal. The output of the mixed signal 2-bit comparator circuit may be less than, equal to (ET), or greater than.

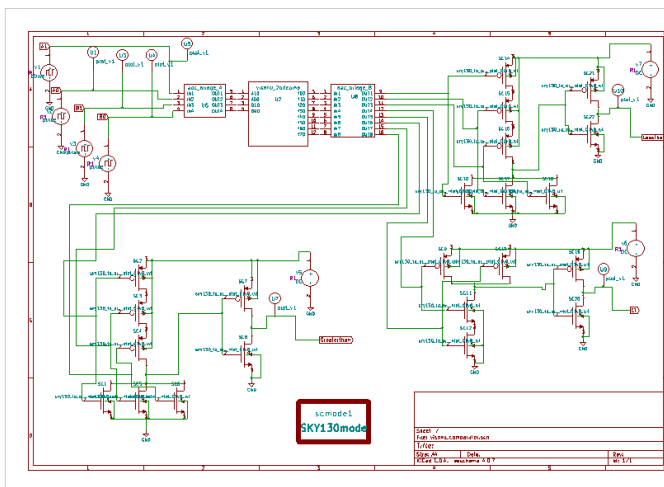## II. Implemented Circuit

Fig. 1. Implemented Circuit Diagram

III. Implemented Circuit Waveforms

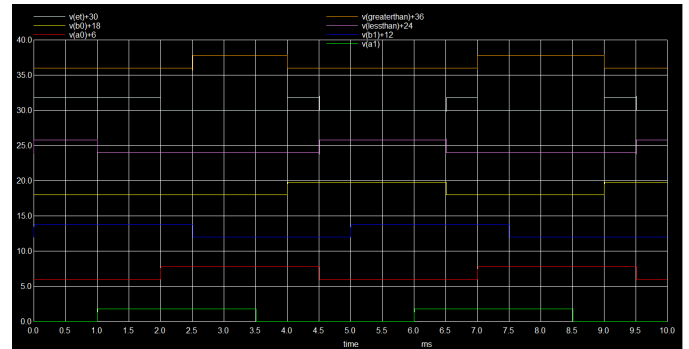Fig.2 depicts waveform of 2-bit magnitude comparator circuit.

Fig. 2. Implemented Waveform

References

[1] Weste, Neil HE, and David Harris. CMOS VLSI design: a circuits and systems perspective. Pearson Education India, 2015.
[2] Mano, M. Morris. Digital logic and computer design. Pearson Education India, 2017.
[3] https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/