4 Bit Asynchronous Up Counter Using JK Filp Flop

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Abstract

In most of the applications counter is used to divide input clock to produce output, the frequency of the output is the divided by n times of input clock frequency. Due to these reasons ripple counters can be used as frequency dividers to reduce a high clock frequency down to a more usable value for use in digital clocks and timing applications. In this paper design of 4 bit asynchronous counter can be simulated using on esim.

1 Reference Circuit Details

As shown in the figure we have four JK flip flop for 4 bit counter and one clock as a clock source as shown in the figure.

Any n bit Asynchronous counter can count $2^n - 1$ possible counting states. In this given circuit will count from 0000(0) to 1111(15) states.

The first flip flop F0 will react at only positive edge of the clock and all other flip flops F1, F2, F3 are react at negative edge of the clock cycle.

The advantage of the using asynchronous counters can be easily built. These Asynchronous counters gives more flexibility for implementation of any mod n counter.

2 Reference Circuit

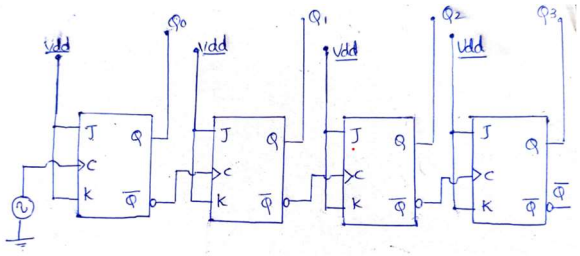

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

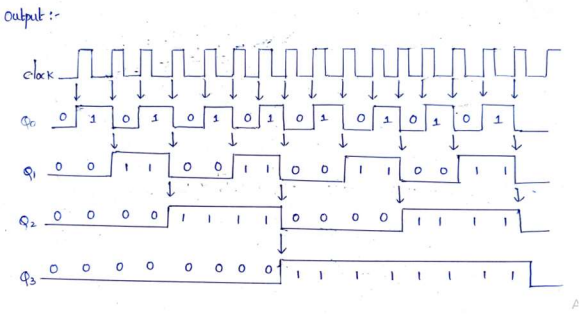

Figure 2: Reference waveform.

References

1. V. Sravaran, V. Kannan, "Low power Asynchronous up counter using CNTFET," *2012 International Conference of computer Application (0975 – 8887) Volume 51– No.2, August-2012.*