Clk_Generator-RVMYTH-DAC mixed-signal circuit Design & Simulations with eSim

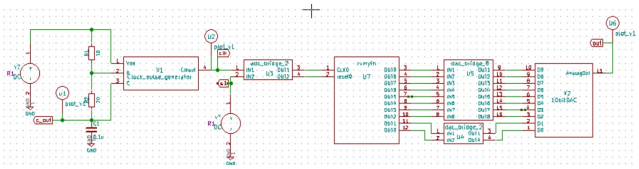
khadija Fahr : Khadija.fahr@googlemail.com

Abstract

This paper presents a result of implementation and simulations of a mixed signal circuit with the open-source EDA tools eSim. First I design and simulate 2 analog circuits *Fahr_clk-gen* and *Fahr_10bitDac *after I simulate the tlv code of my digital circuit *Fahr_rvmyth* by Makerchip and create it s model by Ngveri .Finally I implement my reference mixed signal circuit and simulate it with eSim.

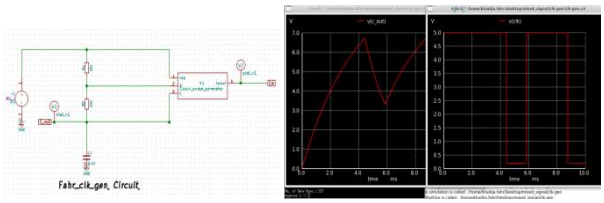
Keywords: RVMyth, DAC, Clk-Gen, eSim, , makerchip,Ngveri,NgSpice

I. REFERENCE CIRCUIT



1 *Fahr_clk_gen * Circuit

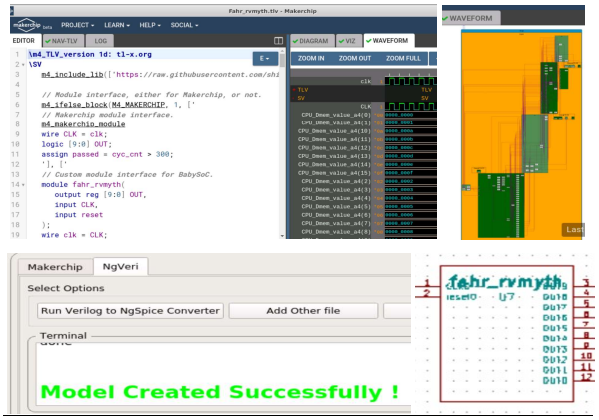
I design a circuit to generate the clk signal by using the subchip clk_pulse_generator from eSim componant, I generate a verilog module for ***Fahr_clk-Gen*** and obtain the analog v(clk) for R1=R2=20K,Vdd=10V ,v(c_out) the plot at the out of capacitor C=0.1u



Design v(c_out) , v(clk)

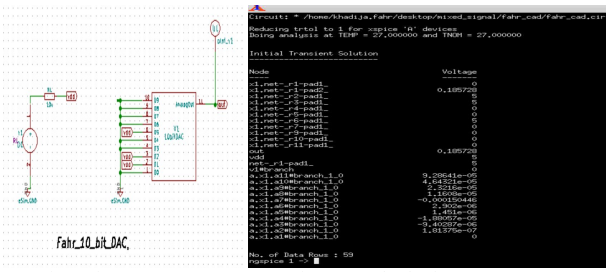
2) *Fahr_rvmyth* circuit

I used the tlv code for rvmyth and edit it succesefly by makerchip and run verilog to NgSpice Converter to create the model ***fahr_rvmyth***



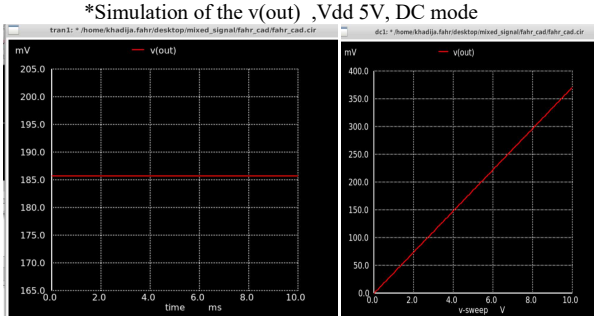
3) *Fahr_10bit_DAC* Circuit

I used the subship 10bit_DAC from library to generate a Netlist verilog module of DAC and obtain the analog v(out) for digital inputs to test it.



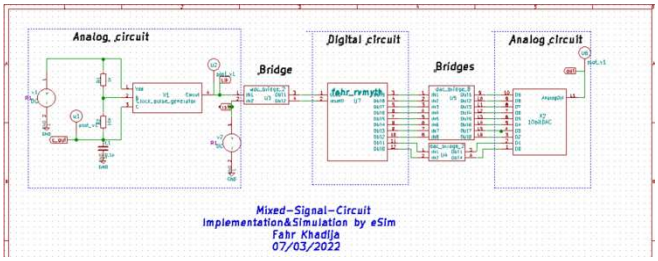
Design of DAC NgSpice calcul of V(out)

*Simulation of the v(out) ,Vdd 5V, DC mode

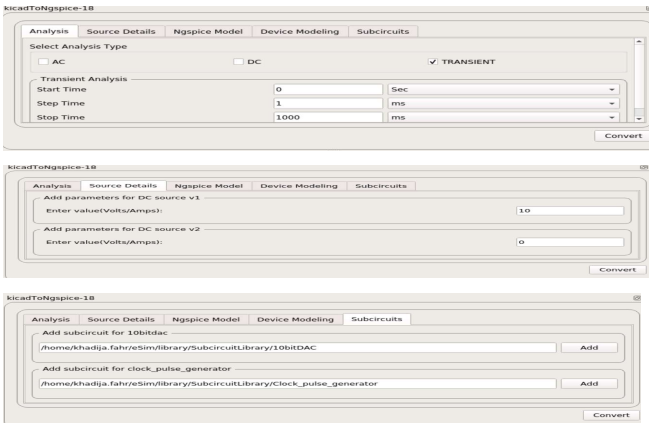


II. DESIGN & SIMULATION OF REFERENCE CIRCUIT

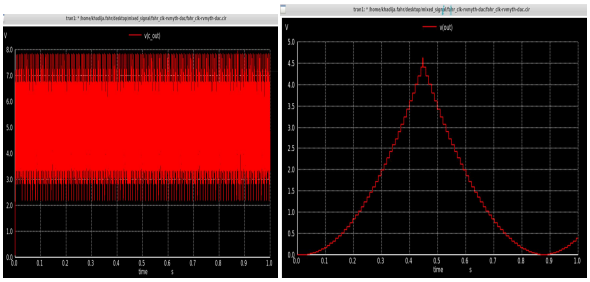
* Implementation with eSim



* Setting of Analysis type –source detail—add Subchips



*Simulation of the reference mixed circuit



REFERENCES

[1] https://github.com/vsdip/rvmyth_avsddac_interface

[2] https://github.com/vsdip/rvmyth_avsdpll_interface

[3] https://esim.fossee.in/circuit-simulation-project/esim-circuit-simulation-run

[4] https://hackathon.fossee.in/esim/