

Resistor-Transistor Logic NOR gate

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Abstract:

As part of this marathon, an RTL NOR gate is designed and simulated with the eSim tool. It's a basic logic circuits in Digital logical families and it is popular for simplicity. It consists of resistors as inputs and transistors as outputs and transistors are used for switching device and emitter of transistor is connected to ground and inputs connected directly to the transistor bases and given to the supply through the resistor R_c (5v/2Amps).

Circuit Details:

In this circuit of 2-input Resistor and 2 transistors. A_{in} and B_{in} are the two inputs, given to the base of two transistors and V_{out} is the output and when both the inputs A_{in} and B_{in} are low then both transistors are in saturated off state and voltage $+V_{cc}$ will appears high at the output V_{out} .

In any one of input either A_{in} or B_{in} is high and logic 1, then transistor input will be turned On and it will make a way so that the supply voltage passes to the ground through the R_c resistor and the transistor and it will be 0v at the output Y and when both the inputs are high, it will operate the transistor to turn on and it will make a path for the supply voltage passes to the ground through resistor R_c and it will be 0v at the output V_{out} .

Implemented Circuit:

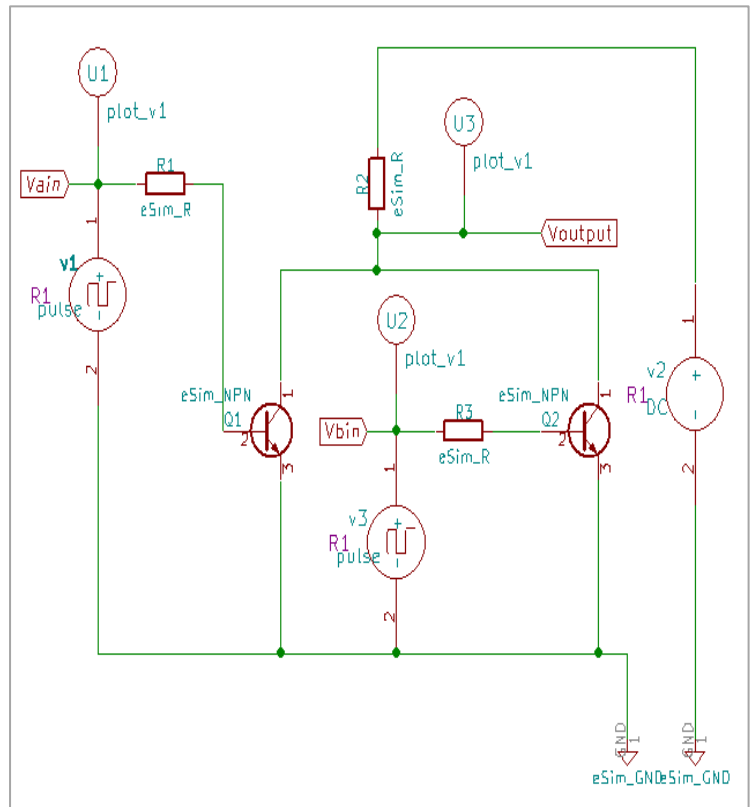


Fig: 1.0 rtl_nor_circuit_using_esim

Truth Table:

A	B	$Y=(A+B)'$
0	0	1
0	0	0
1	1	0
1	1	0

Implemented Waveforms:

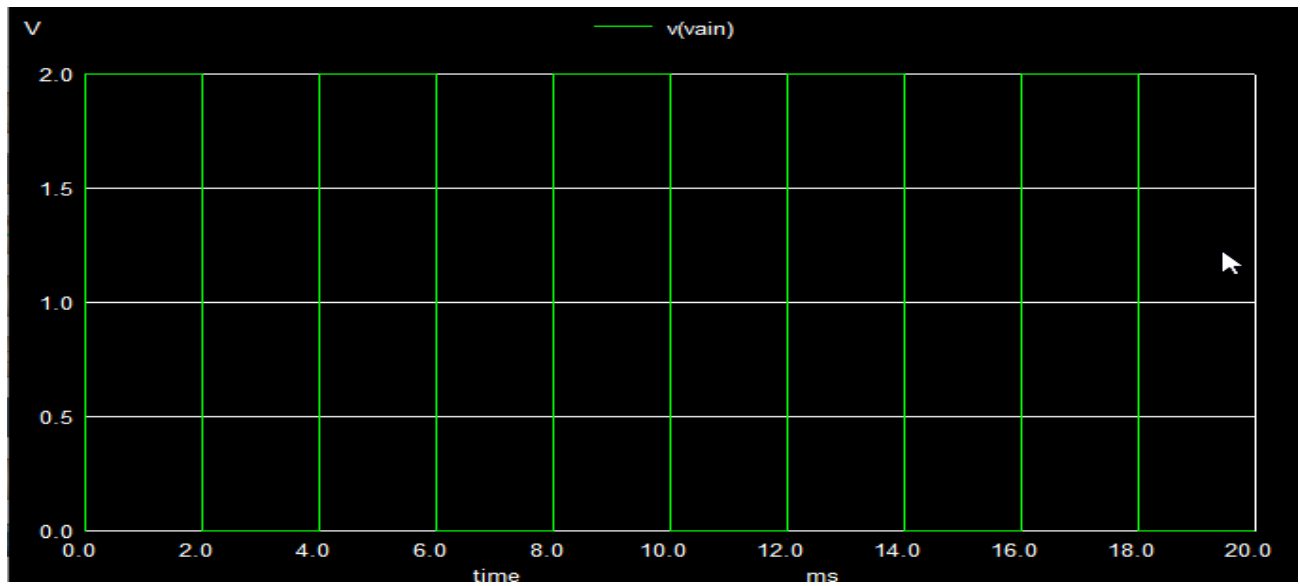


Fig 1.1 VAinput. (2 Amps)

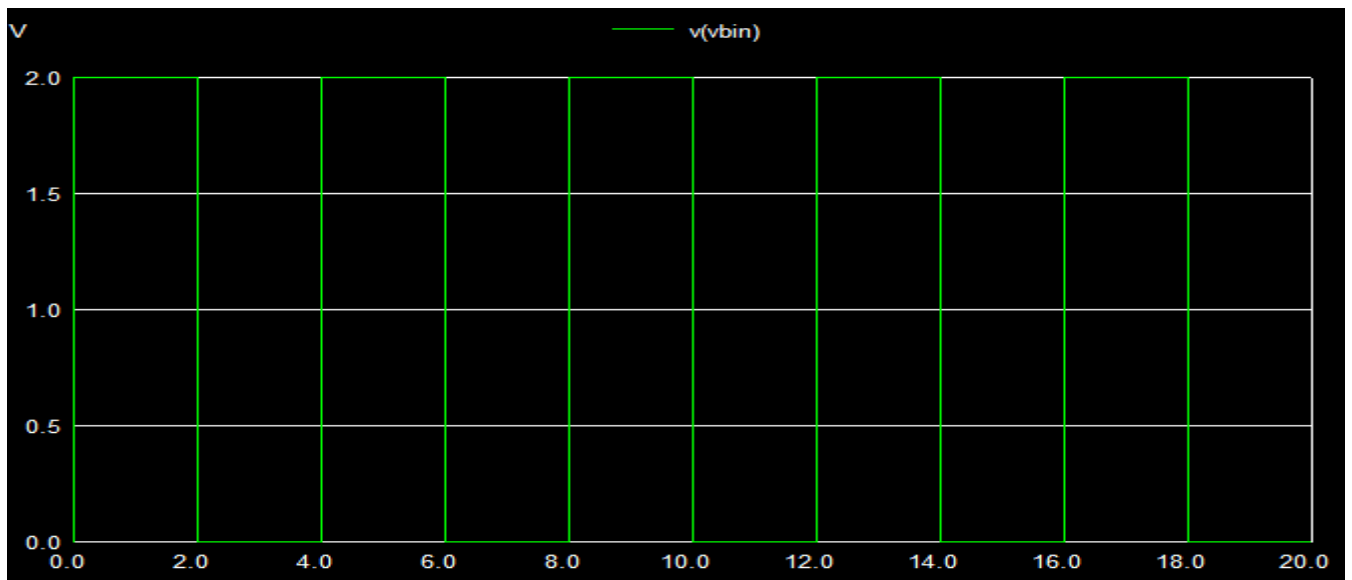


Fig 1.2 VB input (2 Amps)

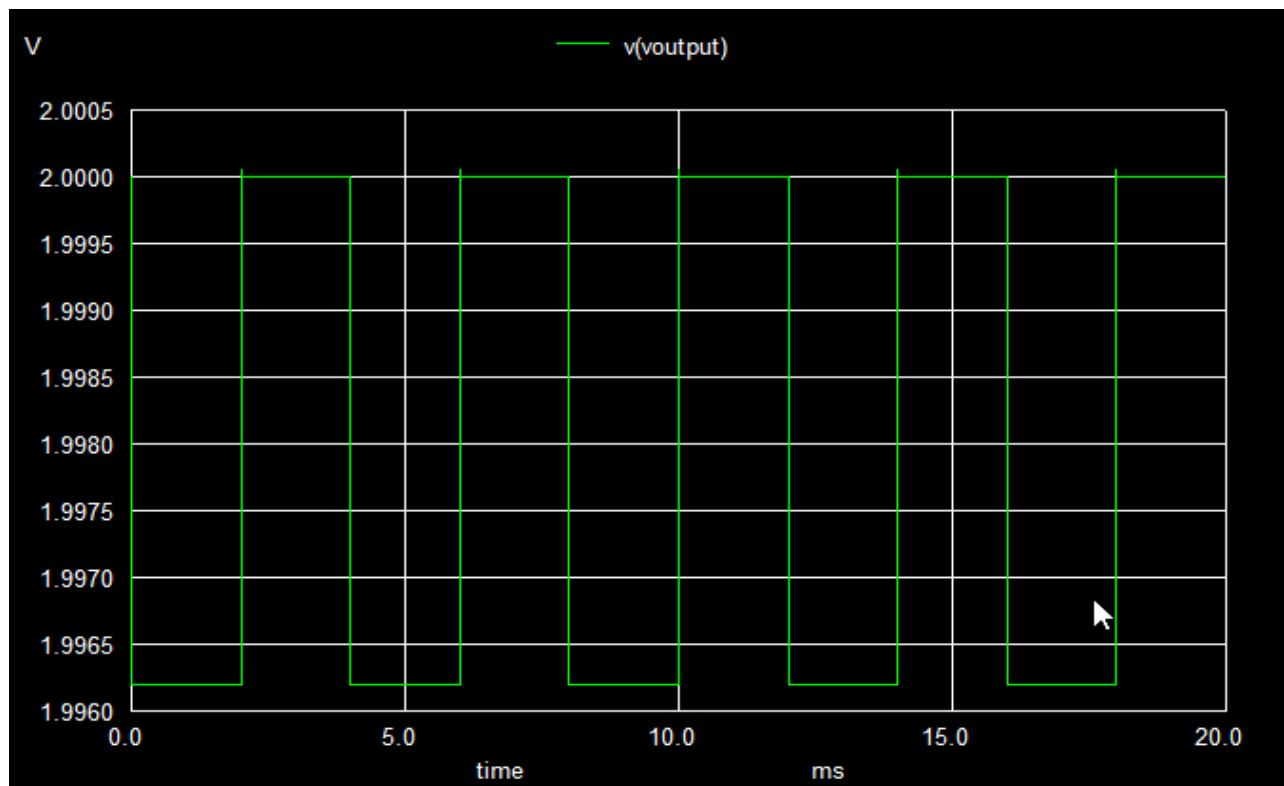
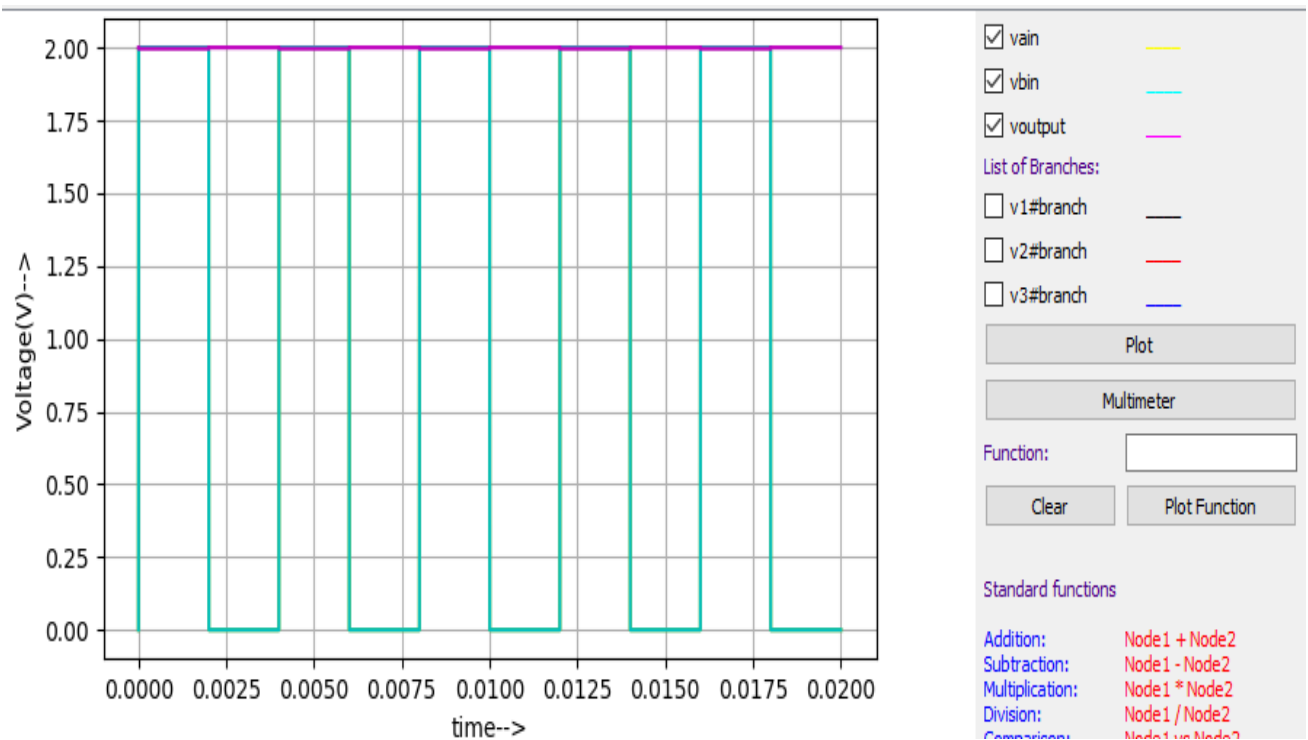


Fig 1.3 V output



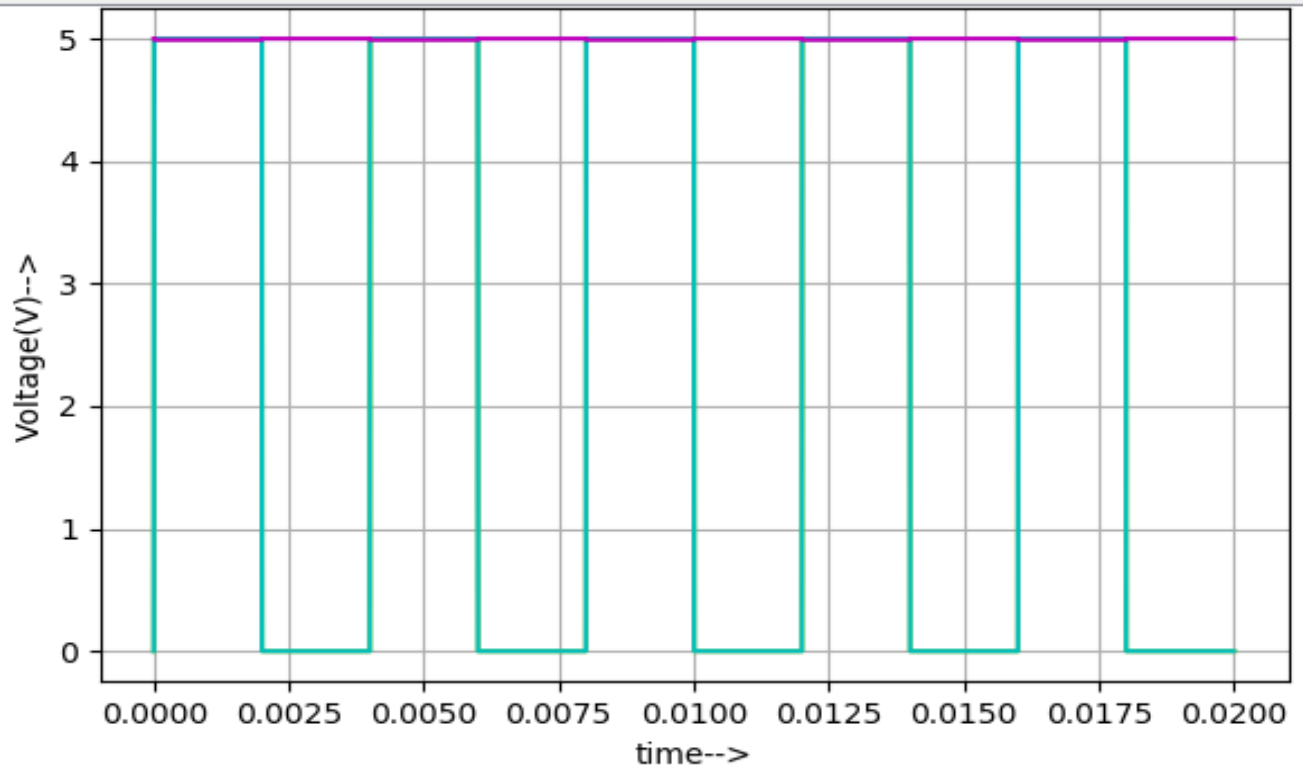
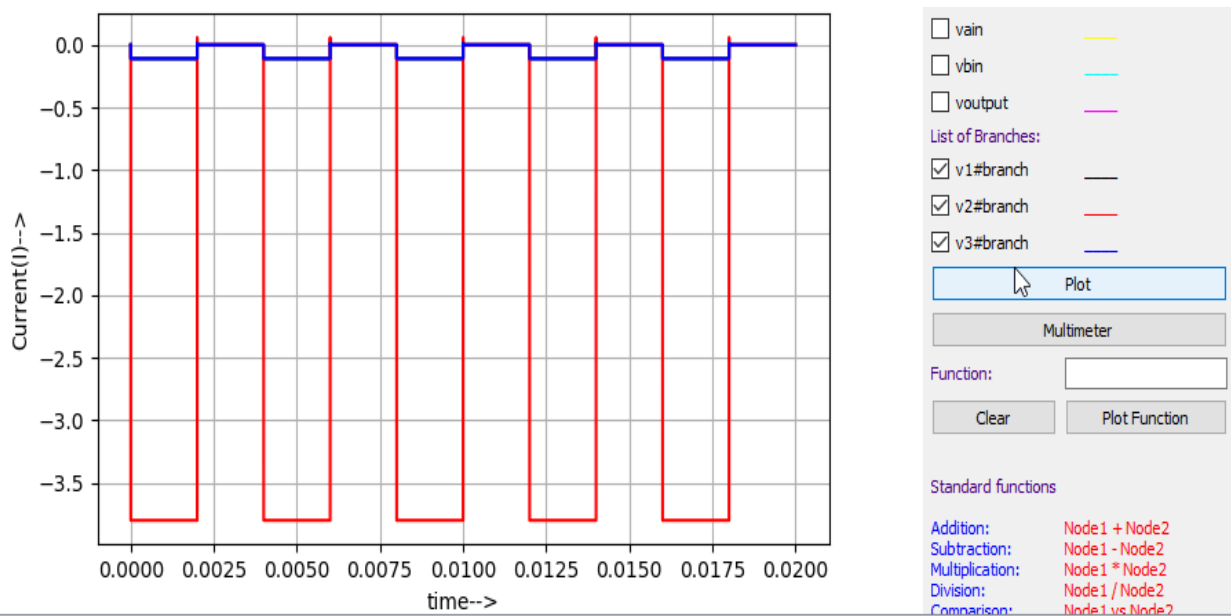


Fig 2.0 Python Plotting of input and output signal (Amps and Voltage)



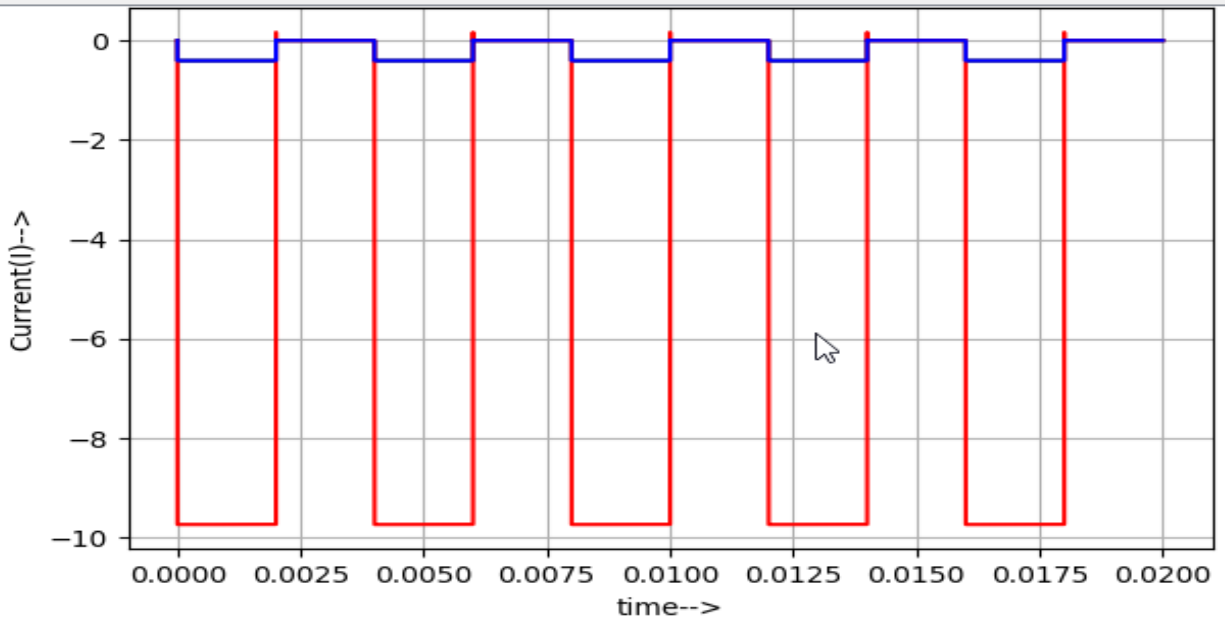


Fig 2.1 Python Plotting of voltage branches (Amps and Voltage)

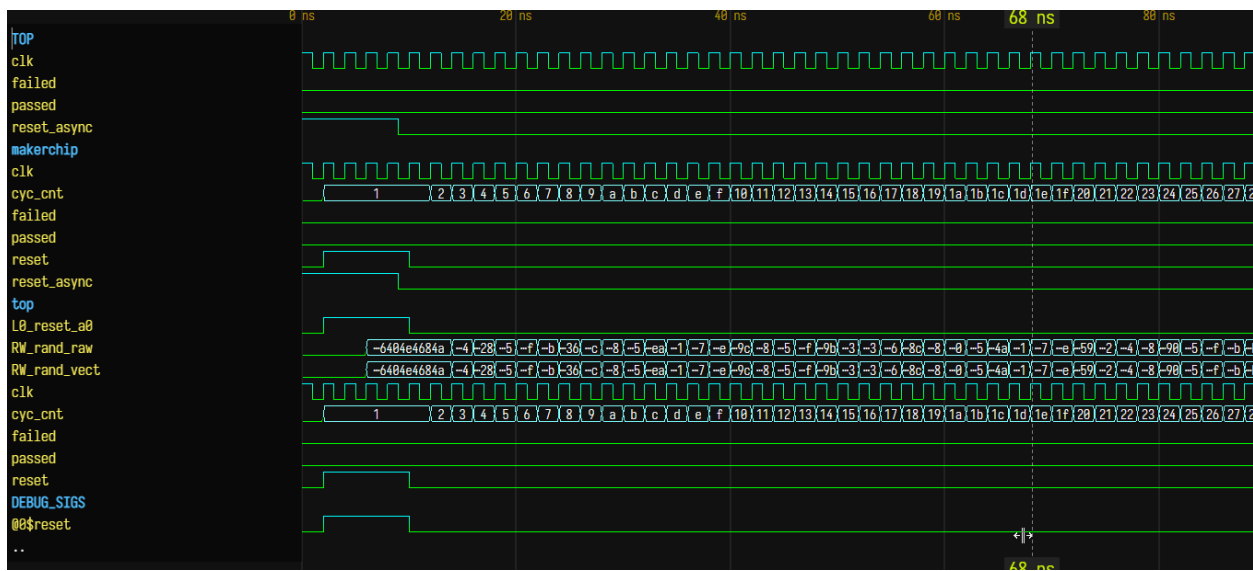
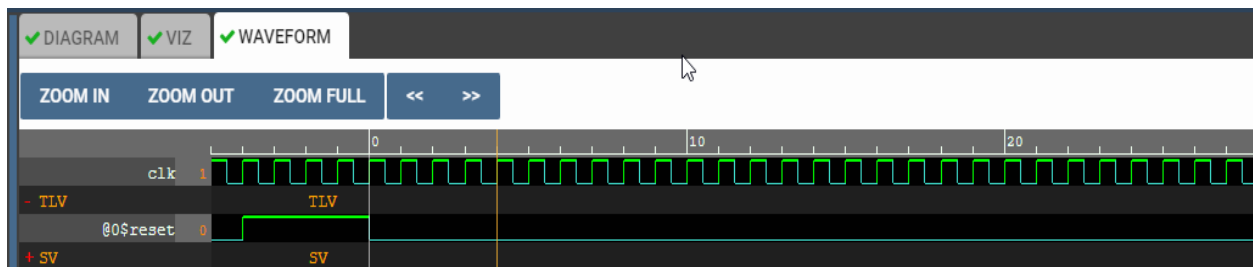
Verilog Code :

```
\m4_TLV_version 1d: tl-x.org
\SV

module rtl_nor_circuit_rawat(output reg O, input X, Y);
always @ (X or Y) begin
    if (X == 1'b0 & Y == 1'b0) begin
        O = 1'b1;
    end
    else
        O = 1'b0;
end
endmodule

// =====
// Welcome! Try the tutorials via the menu.
// =====

// Default Makerchip TL-Verilog Code Template
```



Acknowledgements:

- FOSSEE, IIT Bombay
- Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd.
- Sumanto Kar, eSim Team, FOSSEE

Conclusion:

As a result, we obtain the appropriate waveforms of circuits of rtl_nor gate using eSim and Verilog.

References:

<https://www.electronics-lab.com/article/logic-norgate/>

<https://www.youtube.com/watch?v=Jar8gw7oyGQ>, <https://technobyte.org/verilog-nor-gate/>, <https://electronics-club.com/resistor-transistorlogic-rtl/>