HALF ADDER USING CMOS

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ABSTRACT:

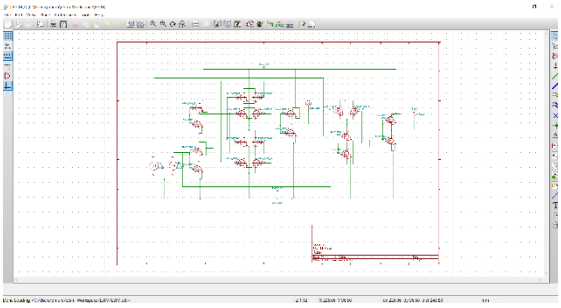
A half adder is a digital logic circuit that performs addition of two single bit binary numbers. Generally, in various types of processors, adders are used to perform arithmetic and logical operations. In this paper, working of half adder is analysed by designing it by using CMOS logic. The comparison has been made between the other circuits on the basis of their power consumption and transistor count. After simulation it is observed that power consumption is lowest when the adder is implemented by transmission gate as compared to CMOS and PTL design styles whereas transistor count is minimum in case of PTL design style. It is also inferred that CMOS gives the best performance out of the three design styles.

Keywords— Power dissipation, CMOS, pass transistor, transmission gate, transistor count

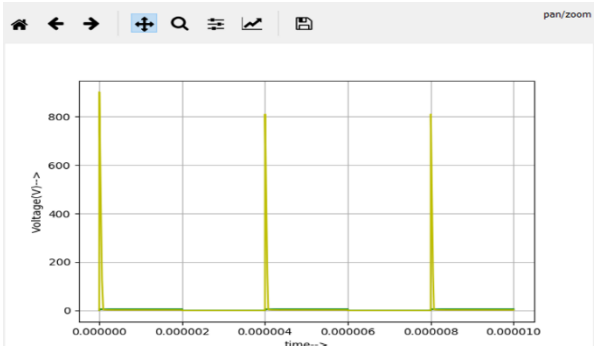
IMPLEMENTED CIRCUIT DETAILS:

Complementary Metal Oxide Semiconductor (CMOS) logic deploys symmetric number of both types of MOSFETs, i.e., pMOS and nMOS. This leads to better performance of any logic circuit since nMOS is strong ‘0’ device and pMOS is strong ‘1’device. Thus, CMOS provides complete ‘1’ and complete ‘0’ logics at the output without any distortion. Half Adder using CMOS modeled using 12 Transistors. Comparison of half adder implemented using Pass Transistor Logic, Transmission Gate Logic and CMOS logic has been reviewed on the basis of power consumption and transistor count.

DIAGRAM:



IMPLEMENTED OUTPUT WAVEFORM:



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