

Cockroft Walton charge pump using NMOS technology

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Abstract

Cockroft Walton charge pump or Cockroft Walton generator is a circuit comprising of a ladder network of NMOS transistors and capacitors, which performs the operation of voltage multiplication. A low amplitude ac signal is used as the input to produce a high dc voltage. This circuit is used in applications where high voltage is required. This circuit also act as a charge pump circuit by pumping the charges towards the capacitors in the ladder network. These capacitors can store the electric charges to increase or decrease the output voltage.

Reference Circuit details

A two stage Cockroft Walton charge pump is presented in this work. The number of stages of this circuit is determined by the number of capacitors between the output and the ground. Here NMOS transistors act as diodes. The voltage across each stage is equal to two times the peak value of the input ac voltage in a half wave rectifier.

Let us consider that the input ac voltage is V_i and let the peak value be V_p . The capacitors are uncharged initially. As the input ac voltage flows in the circuit and attains the negative peak $-V_p$, the capacitor C_1 gets charged to V_p as the current passes through NMOS transistor N_1 . When the polarity of the input signal is reversed and reaches the positive peak V_p , the current flows from capacitor C_1 to capacitor C_2 through NMOS transistor N_2 and the capacitor C_2 is charged to a voltage equal to two times of V_p . As the polarity of the input signal is reversed again, the current flows from capacitor C_2 to capacitor C_3 through NMOS transistor N_3 , charging the capacitor C_3 to a voltage of two times of V_p . Again, as the input signal changes its polarity, current flows from capacitor C_3 to capacitor C_4 through NMOS transistor N_4 , charging the capacitor C_4 to a voltage equal to twice of V_p . Each time the input voltage changes its polarity, current flows through the ladder network until all the capacitors are charged. Capacitor C_1 is charged to V_p whereas the other three resistors are charged to voltage equalling twice of V_p .

As the output measures the voltage of series combination of capacitor C_2 and capacitor C_4 , the output voltage equals four times of V_p .

Implemented Circuit

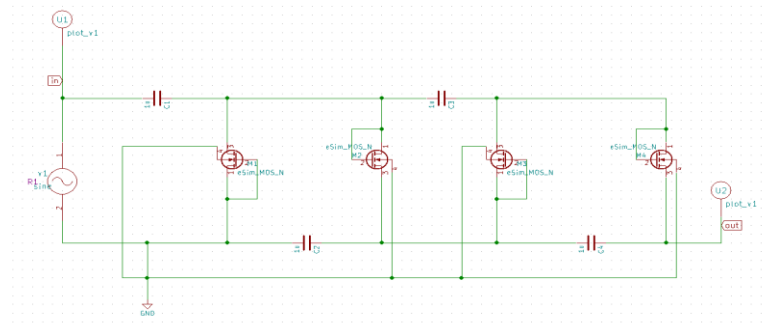


Figure 1. Implemented Circuit Diagram

Implemented waveform

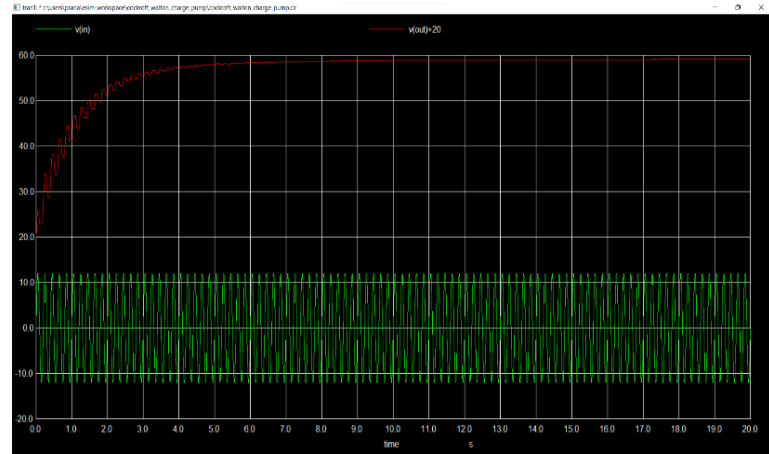


Figure 2. Implemented waveform

References

- [1] Vipul V.Nandedkar, Nigroth B.Narnaware, "Design and Implementation of a Cockroft-Walton voltage Multiplier circuit", 2017 International Journal of Engineering Development and Research (IJEDR), Volume 5, Issue 2, ISSN: 2321-9939.