

DESIGN OF FLASH TYPE ADC /PARALLEL COMPARATOR TYPE ADC
MANOJ KUMAR SINGH
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY,ALLAHABAD
28 FEBURARY 2022

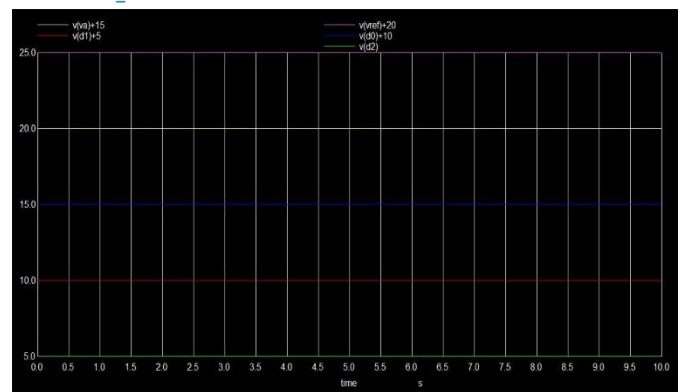
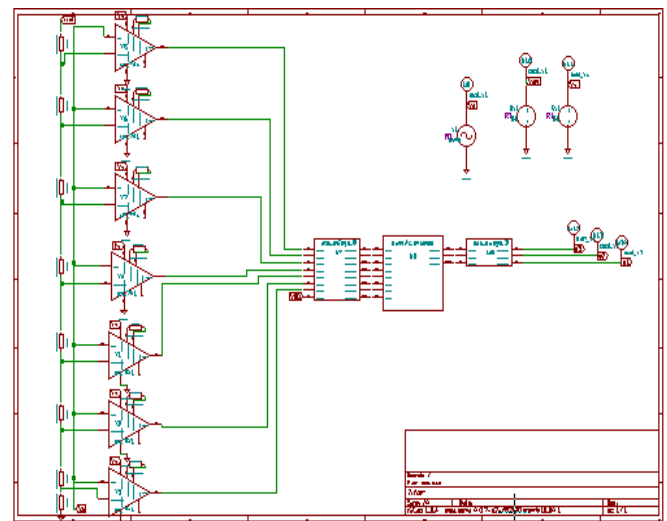
Abstract: Analog to Digital converters are essential in all communication and signal processing applications. Among all ADC'S Flash ADC has a high speed conversion rate. It has a capacity of sampling a signal up to Giga Bites. The conventional Flash ADC contains the resistor ladder network, comparator, and encoder. Due to the use of resistor ladder network in conventional Flash ADC static power consumption is more to overcome this issue, new 3-Bit Flash ADC has been proposed. The proposed ADC is consists of sample and hold (S/H) circuit, threshold modified comparator circuit and priority encoder. The design is implemented with a supply voltage of 1.8 V and clock frequency of 1M Hz.

Keywords - ADC, sample and hold(S/H) circuit, TMCC, Threshold voltage, Multiplexer, encoder and Flash ADC

REFERENCE CIRCUIT DETAILS

figure shown a 3 bit flash type A/D converter which requires $(2^3-1)=8$ comparators. The analog input which is to be converted is connected to the non-inverting terminal. Input terminal of comparator where as the inverting input terminals of op-ams are connected to a set of reference voltage provided by voltage divider that divides it into 7 equal increment levels.

Each level is compared to the analog input by a voltage comparator. All comparators O/Ps are connected to a priority encoder, which produces a digital o/p corresponding to the i/p having highest priority. Thus, the digital o/p represents the voltage that is closest in value to the analog input.



REFERENCES

1. Swarupa B N, Dr. Vijaya Prakash A M, Kumaraswamy K V "Implementation of a 3-bit Flash ADC using TIQ Modified Comparator Circuit and NORROM based Encoder" International Journal of Innovative Research in Computer and Communication Engineering Vol. 5, Issue 5, May 2016.
2. Mayur. S. M, Siddharth R. K, Nithin Kumar Y. B, Vasantha M. H "Design of Low Power 5-bit Hybrid Flash ADC" 2016 IEEE Computer Society Annual Symposium on VLSI.