

# Design of JK flip flop using mixed signals

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**Abstract-** A flip flop is an electronic circuit which consists of two stable states and these can be used to binary data. There are different types of flip flops like SR, JK, D and T flip flops. In this paper we are concentrating on designing a JK flip flop using mixed signals i.e. both analog and digital signals.

## 1. Reference circuit details

The SR flip flop has lots of advantages but it has the following two switching problems: the first is that when both Set and Reset inputs are set to 0, this condition is always avoided, and the second one is that when the Set or Reset input changes their state while the enable input is 1, the incorrect latching action occurs. The JK flip flop removes these two drawbacks of SR flip flop.

Here, we provide the binary input to the JK flip flop by using an Analog to Digital converter at the beginning of the circuit and the output of JK flip flop will again be converted to Analog signal by using a Digital to Analog converter. In this way we can design a JK flip flop by using mixed signals.

The working of JK flip flop is same as that of SR flip flop. The difference is this time the JK flip flop has no invalid state when both the inputs are high. The JK flip flop is basically a gated SR flip flop with additional clock input which prevents the invalid state. Two AND gates are connected in the circuit as we can see from the circuit diagram and the third input to each AND gate is connected to outputs of Q and Q bar.

Truth Table

J	K	CLK	Q
0	0	↑	$Q_0$ (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)

## 2. Implemented circuit

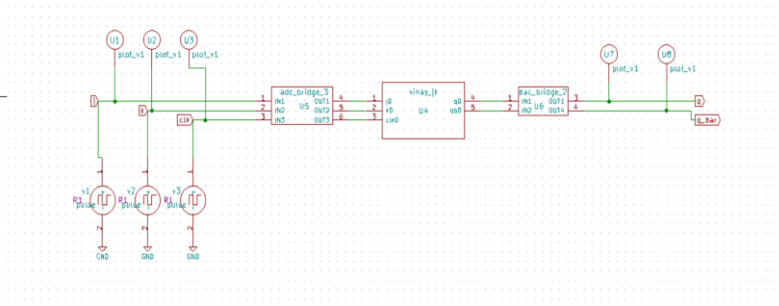


Fig-1: JK flip flop in mixed signals

## 3. Circuit waveforms

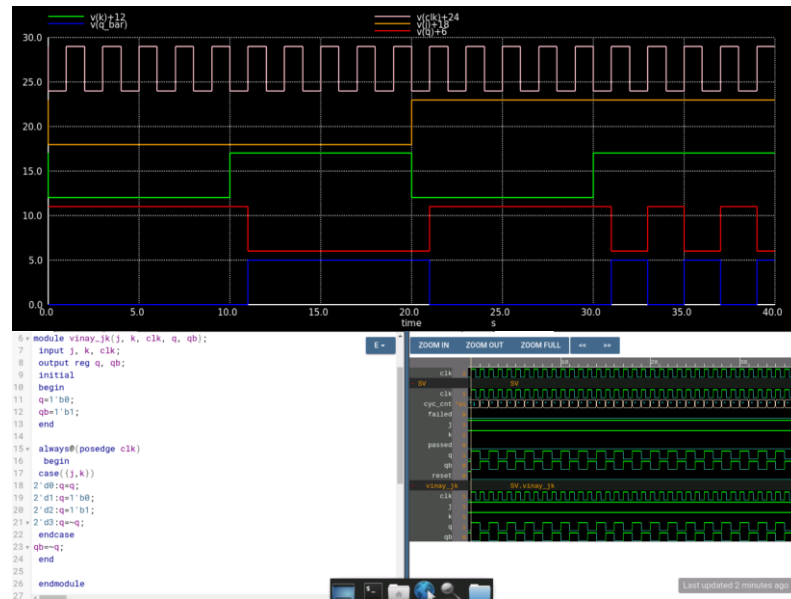


Fig-2: Simulation result waveforms

## References

- [1] V.T.Phyne, Fundamentals of Digital Systems Design, NJ, Englewood Cliffs: Prentice-Hall, pp. 217-245, 1973.
- [2] J.Millman and C.C.Halkias, Integrated Electronics: Analog and Digital Circuits and Systems, New York: McGraw-Hill, pp. 627-632, 1972.