

# Implementation of Conventional Full Adder Architecture Using esim Tools

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## Abstract

This article proposes a 28T CMOS Full Adder circuit. The design analysis is verified by Circuit Schematic and Waveforms using esim and ngspice (ngver) Software Platform. The design is implemented using 180nm CMOS technology.

A single bit full adder is a basic block that performs complex arithmetic logic circuits like addition, division, multiplication, and exponent circuits. The addition is the most fundamental arithmetic operation, widely used across various components as subtractors and multipliers as a basic unit.

## 1 Reference Circuit Details

This article reports the design analysis of 1-bit full adder cells implemented using CMOS logic. The 1-bit full adder is a static CMOS with complementary nmos and pmos. This one-bit adder is based on a typical CMOS structure with pull-down and pull-up networks, utilizing nmos and pmos transistors. Because the nmos transistors in static CMOS only need to pass 0's and the pmos transistors only need to pass 1's, the output is always forcefully pushed, and the levels are never degraded. This is referred to as a completely recovered logic gate. The pull-up network is the inverse of the pull-down network. Inputs for one 1-bit adder are A, B, and Cin. and the outputs are defined as sum and carry. Below a simple truth table is being implemented for a 1-bit adder.

## 2 Reference Circuit

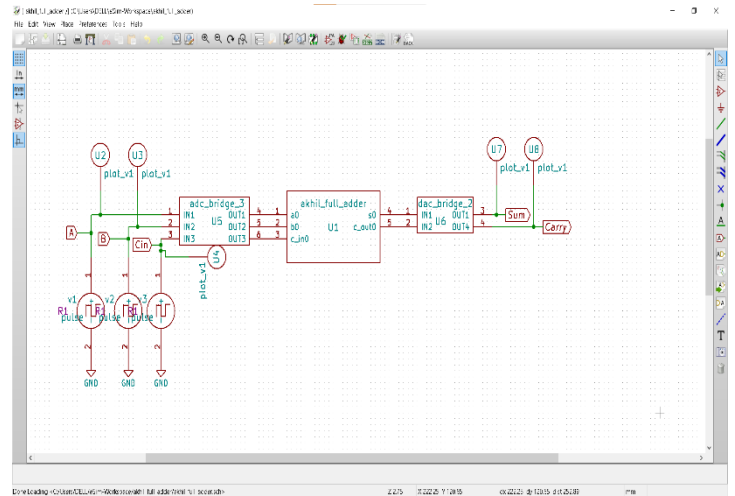


Figure 1: Reference circuit diagram.

## 3 Reference Circuit Waveforms

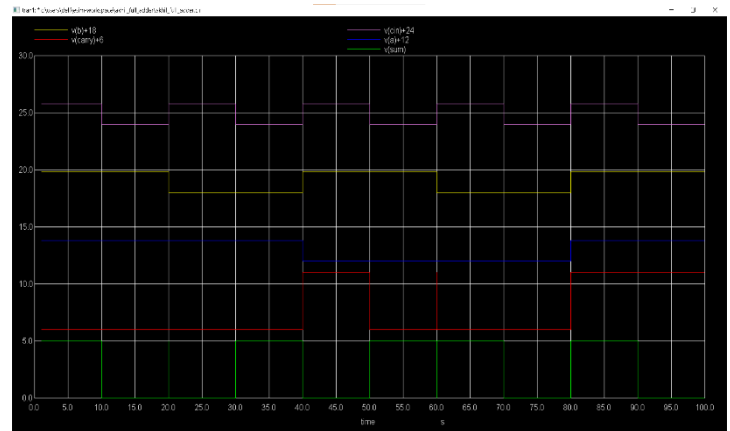


Figure 2: Reference waveform.

## 4 References

- [1] N. Weste, and K. Eshraghian, "Principles of CMOS VLSI Design: A Systems Perspective," Second Edition, Addison Wesley, 1993.
- [2] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEE Proceedings - Circuits Devices and Systems, vol. 148, pp. 19-24, Feb. 2001.