

# RVMYTH MIXED SIGNAL

YOGAPRIYA.B, EASWARI ENGINEERING COLLEGE, CHENNAI  
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## ABSTRACT:

In this development of processor based on the open-source RVMYTH mixed signal circuit is presented. This processor is designed for targeting low-cost embedded devices. A RISC-V development and validation framework with assembling tools. The resulting processor is a single core, in-order, RISC-V processor with low hardware complexity.

The proposed processor is implemented in Verilog. RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration.

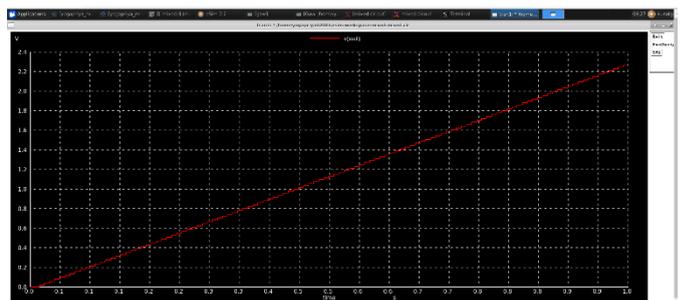
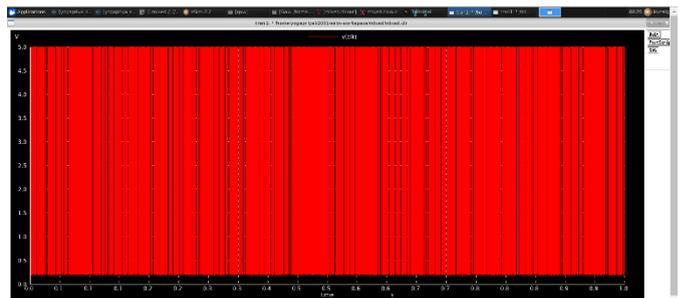
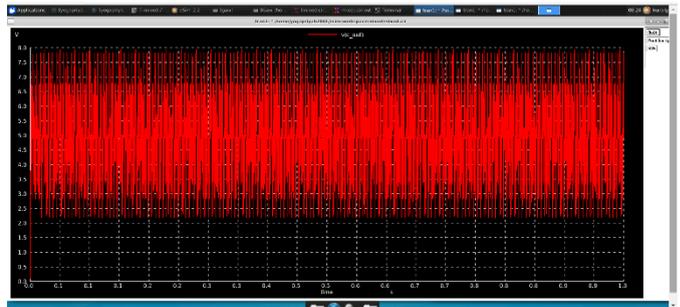
## 1. CIRCUIT DETAILS:

As shown in the figure we have analog circuit and digital circuit in which altogether formed a mixed circuit signal in the RVMYTH mixed signal circuit.

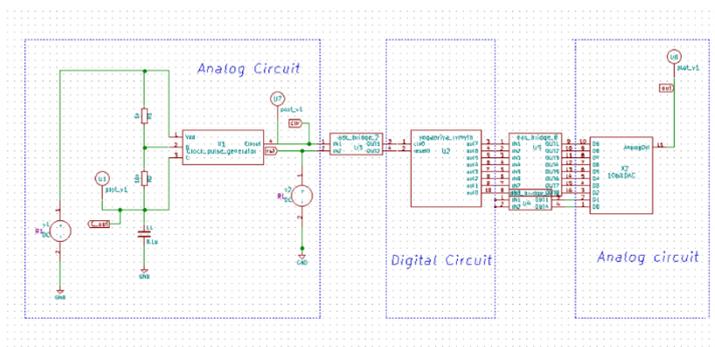
The analog part consists of a clockwise generator connected to resistor capacitor and finally all this grounded. Digital circuit consists of digital board. In between analog and digital circuit ADC and DAC bridges are used as a connector between analog and digital circuit which together forms a mixed signal circuit.

The purpose of this project is to integrate rvmyth (RISC-V) with digital to analog converter (DAC) and perform simulation using end-to-end open-source EDA tools.

## 3. IMPLEMENTED WAVEFORM:



## 2. IMPLEMENTED CIRCUIT



## 4. REFERENCES:

- <https://www.ics.com/blog/what-risc-v-and-why-it-important>.
- <https://www.semanticscholar.org/paper/A-compactfunctional-verification-flow-for-a-RISC-V-MolinaRobles-SoleraBola%3%B1os/bc7b683cd6b3f9a387bac9bbfe4166b6e7f6095d>