Experiment No 5.

JFET Common Source Amplifier

1. Theory:-

The common source circuit provides a medium input and output impedance levels. Both current and voltage gain can be described as medium, but the output is the inverse of the input, i.e. 180° phase change. This provides a good overall performance and as such it is often thought of as the most widely used configuration. Common source FET configuration is probably the most widely used of all the FET circuit configurations for many applications, providing a high level of all round performance.

The input signal enters via C1.This capacitor ensures that the gate is not affected by any DC voltage coming from the previous stages. The resistor R1 holds the gate at ground potential. The resistor R2 develops a voltage across it holding the source above the ground potential. C2 acts as a bypass capacitor to provide additional gain at AC. The resistor R3 develops the output voltage across it, and C3 couples the AC to the next stage whilst blocking the DC.

2. Schematic Diagram:-

The schematic diagram of JFET CS amplifier circuit in eSim is as follows,

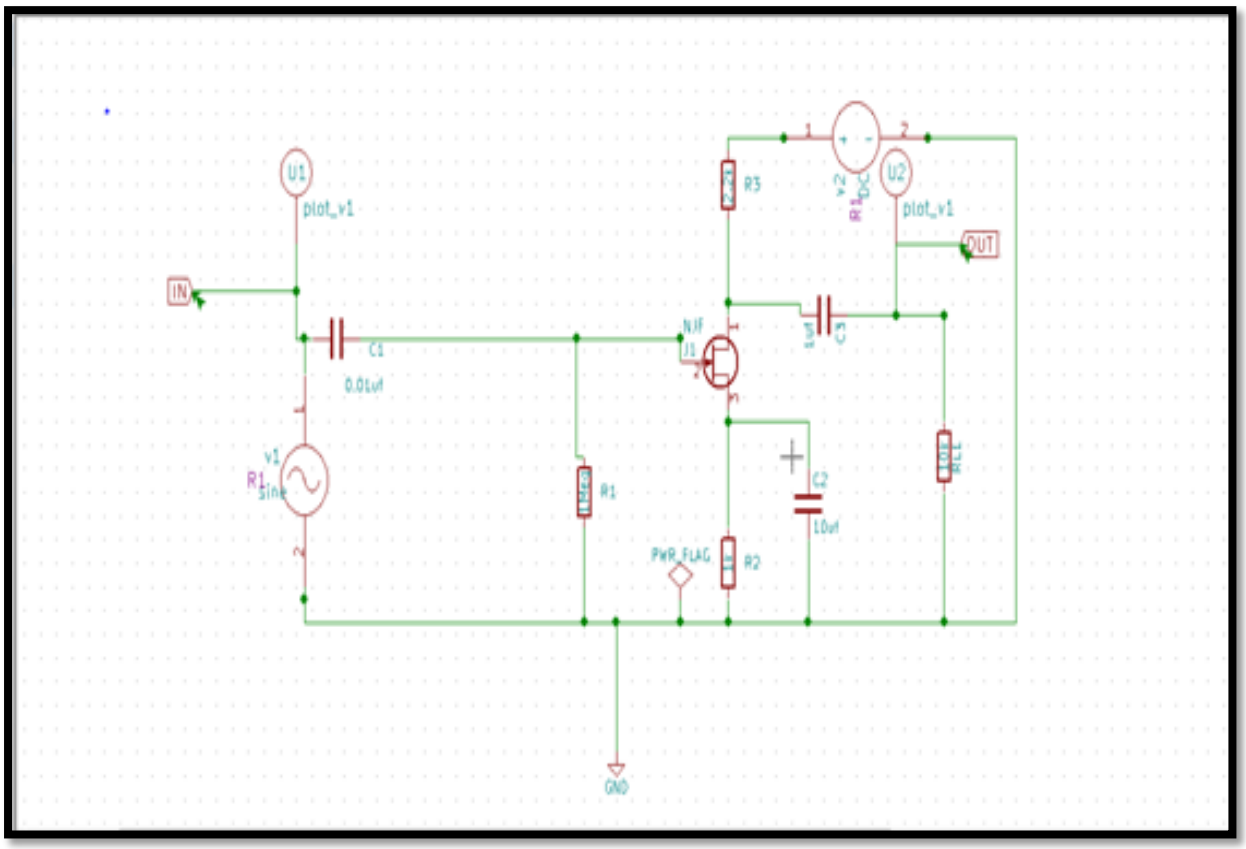

Figure 1. Schematic Diagram of JFET CS amplifier Circuit

3. Simulation Results:

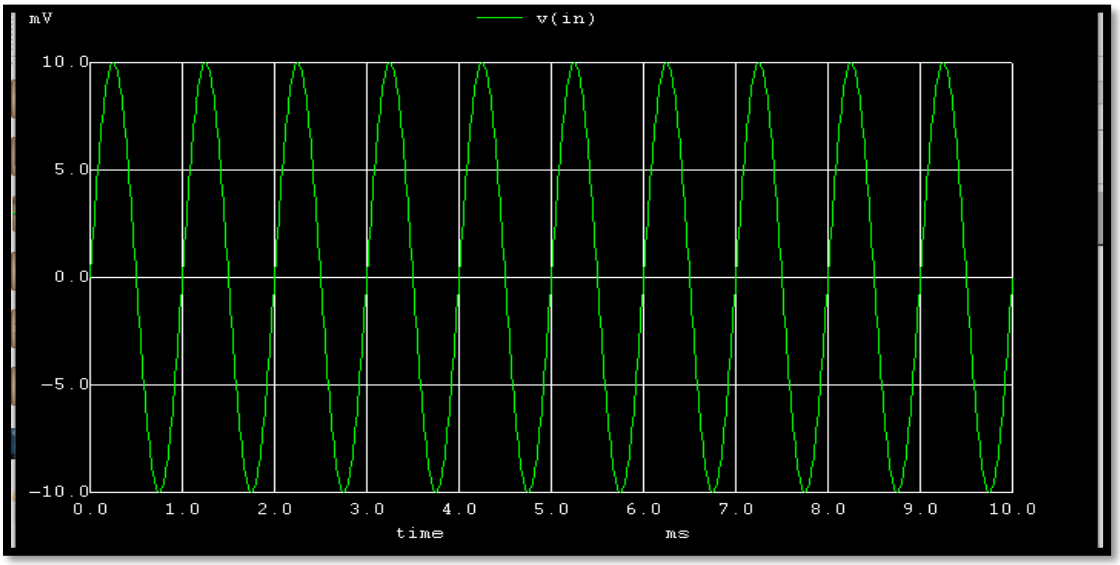

Figure 2: Ngspice Input Plot

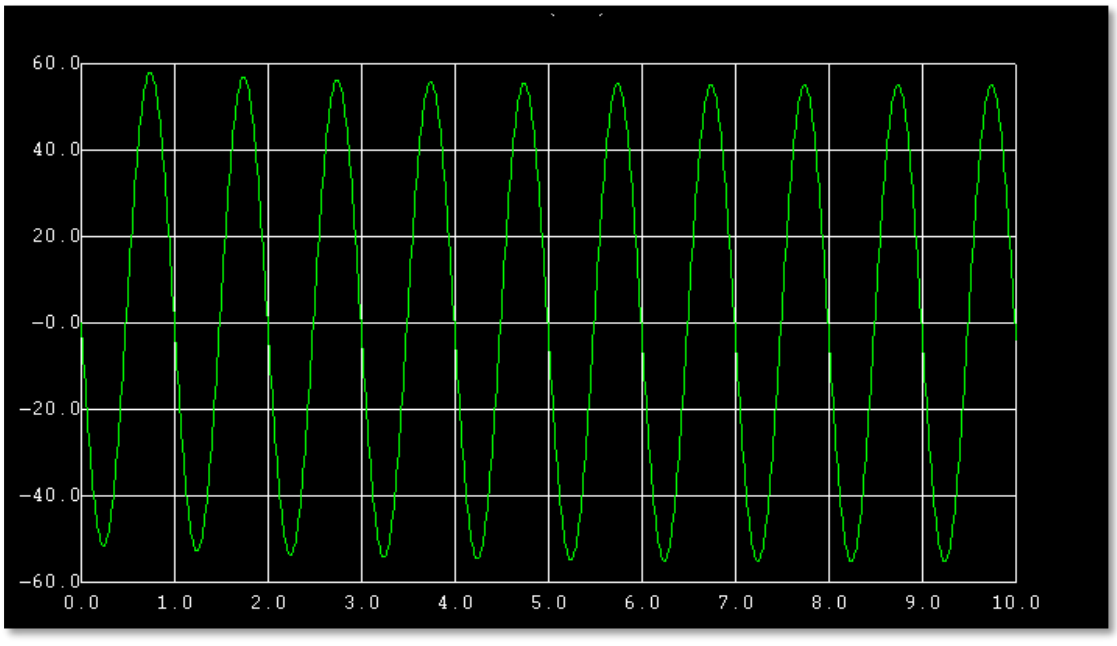

Figure 3: Ngspice Output Plot

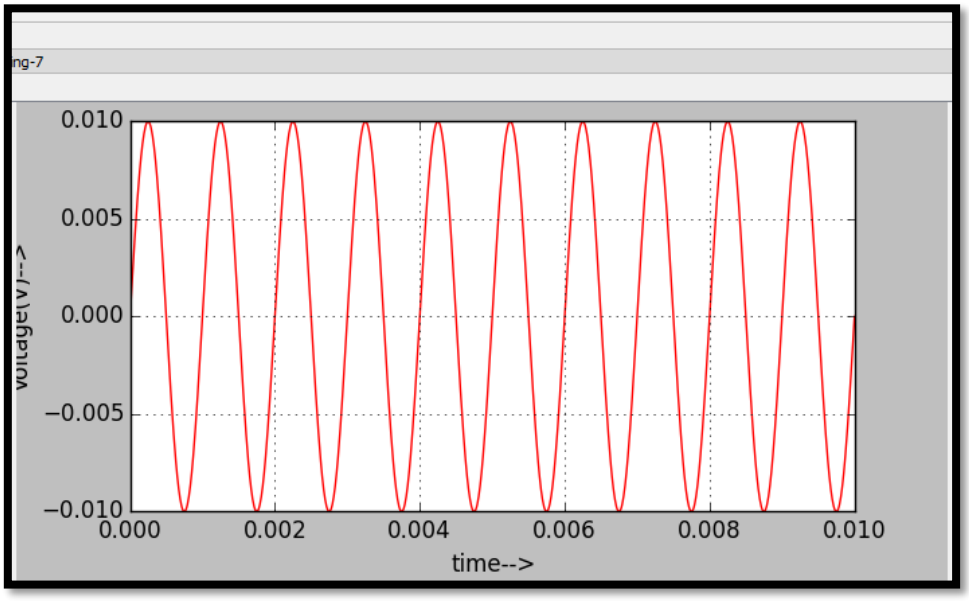

Figure 4: Python Input plot

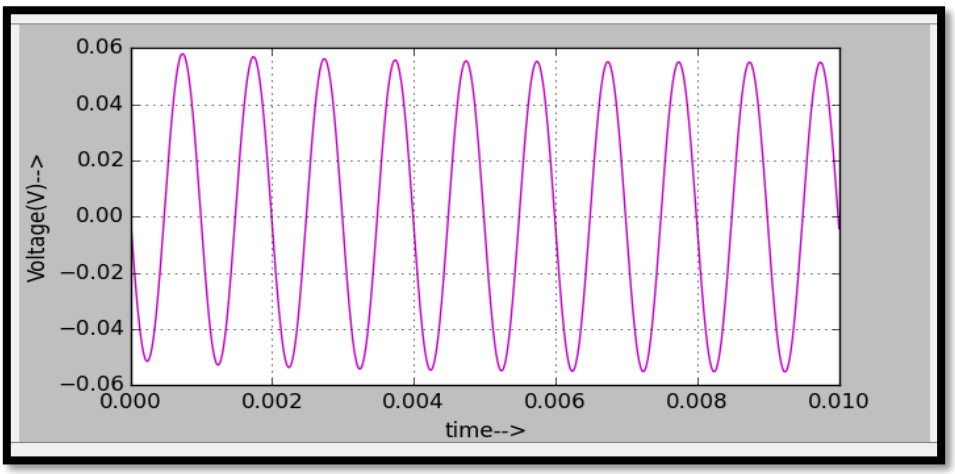

Figure 5: Python Output plot

4. **Conclusion :-** Thus we have studied JFET CS amplifier circuit using eSim and got the appropriate wave forms.

5. **Reference:-**

http://tiij.org/issues/issues/winter98/electronics/huffine/csamp.html.

By,

Priya C Mule , Debajani Mahanta,

Ramrao Adik Institute of Technology,

Nerul - 400706