Design and Analysis of two input NAND gate

MANJUNATHA, yenepoya institute of technology

March 22, 2022

Abstract

The paper constitutes of the modeling of two input NAND gate. The modeling includes schematics design and analysis of NAND gate. In digital electronics, a NAND gate is a logic gate which produces an output which is false only if all its inputs are true. NAND gate is the combination of AND gate and NOT gate. It has the capability to perform the operations of three logic gates such as OR, AND gate and NOT gate. The outputs of AND gate and NAND gates are inverse to each other. NAND gates can also be used to produce any other type of logic gate function, and in practice the NAND gate forms the basis of most practical logic circuits.

1 Circuit Details

The CMOS NAND gate consists of two PMOS transistors and two NMOS transistors. In the figure, the two PMOS transistors are connected in parallel pattern and the two NMOS transistors are connected in series pattern. If either input A or input B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from output to Ground. But at least one of the PMOS transistors will be ON, creating a path from output to VDD. Hence, the output will be high. If both inputs are high, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be logic low. Notice how transistors PMOS1 and NMOS1 resemble the series connected complementary pair from the inverter circuit. Both are controlled by the same input signal ,the upper transistor turning off and the lower transistor turning on when the input is high, and vice versa. Notice also how transistors PMOS2 and NMOS2 are similarly controlled by the same input signal, and how they will also exhibit the same on or off behaviour for the same input logic levels. The upper transistors of both pairs PMOS1 and PMOS2 have their source and drain terminals paralleled, while the lower transistors NMOS1 and NMOS2 are series connected. What this means is that the output will go high if either top transistor saturates, and will go low only if both lower transistors saturate.

2 Implemented Circuit

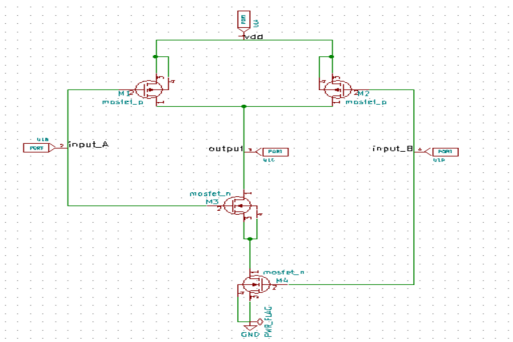

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] B. S. Mukesh kumar, Jagpal Singh Ubhi. Analysis of cmos based nand and nor gates at 45 nm technology. https://www.researchgate.net/publication/316548029.