CMOS Transmission Gate

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Abstract

In this paper, we see that a MOSFET can be used as voltage-controlled switch as the channel created by high gate-to-source voltage allows current to flow between the source and drain terminals. A transmission gate is a combination of both pMOS and nMOS transistor, connected in parallel with an inverter. CMOS transmission gates can be used to switching both analog and digital signals to be conducted in both directions or block by a control signal with almost any voltage potential. It operates as a bidirectional switch which is controlled by a third connection called the control C. Thus, the transmission gates are helpful in being used as an electronic switch, analog multiplexer, and logic circuits.

1 Circuit Details

The CMOS Transmission Gate consists of one PMOS and NMOS and a control signal. It uses the complementary properties of NMOS and PMOS and thus the control signals is complementary.

When the control=0(LOW), both the NMOS and PMOS transistors are cut-off, and the switch is open. In this case, the gate-source voltage at n-channel MOSFET is negative while at p-channel MOSFET its positive. Accordingly, neither of the two transistors will conduct and the transmission gates turns off.

When the control=1(HIGH), both the transistors are biased into conduction and the switch is closed. They provide a low resistance path as the substrate terminal is not connected to the source terminal, the drain and source terminals are almost equal, and the transistors start conducting.

The substrate terminal of the nMOS transistor is connected to ground and the substrate terminal of the pMOS transistor is connected to VDD. The input is logic high (Vin=Vdd). Thus, the I/O characteristics can be observed as a function of Vout. The nMOS transistor will be turned off for Vout > VDD - VT,n and will operate in the saturation mode for Vout < VDD - VT,n. The pMOS transistor is in saturation for Vout < IVT,pI and it operates in the linear region for Vout> IVT,p|. It remains tunred on regardless of Vout. Thus, a transmission gates can be operated in three regions based on the output voltage level. The total current flowing throught it is the summation of nMOS and pMOS drain current.

2 Implemented Circuit

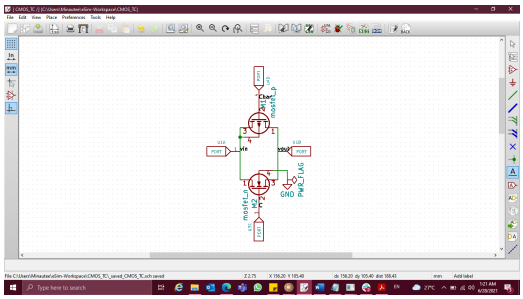

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

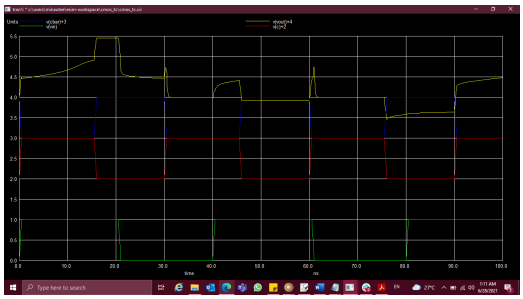

Figure 2: Implemented waveform.

References

[1] D. N. Bhattu. Transmission gate schematic & layout. https://www.youtube.com/watch?v=oej4slig508&t=952s.

[2] I. M. A. M. R. K. P. B. V. K. R. MUPPIDI. Introduction to vlsi design and testing. http://web.engr.uky.edu/ elias/projects/08.