Cmos XNOR gate

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Abstract

The paper constitutes of the design and analysis of XNOR gate using CMOS. The XNOR gate is a digital logic gate whose function is the logical complement of the exclusive OR gate. Logically, an XNOR gate is a NOT gate followed by an XOR gate. The XOR operation of inputs A and B is (A xor B), therefore, XNOR operation those inputs will be (A xnor B) That means the output of the XOR gate is inverted in the XNOR gate. In the XOR gate operation, the output is only 1 when only one input is 1. The output is logical 0 when both inputs are the same, meaning they are either 1 or 0. But in the XNOR gate, the inverse is true. Hence the output is 0 when only one input is 0, and the output is 1 when both inputs are the same.

1 Circuit Details

In static method, the XNOR gate requires more transistors to implement. XNOR gates has 4 Fan in and one Fan out .Static CMOS XNOR gate is shown in figure .Complementary CMOS uses dual networks to implement a given function . A first part consists solely of complementary pullup (PMOS) network while a second part consists of pull-down (NMOS) networks. This technique is popular and produces results that are widely accepted but it requires more numbers of CMOS transistors. The circuit operates with full output voltage swing. In order to design 2-input XNOR gates for equal rise and fall time, it is necessary to first design an inverter with equal rise and fall time. This involves compensating for the difference in electron and hole mobilities. For silicon material, the electron mobility is about 2.5 to 3 times greater than the hole mobility. Therefore, to have equal rise time and fall time in an inverter, we must choose the W/L ration of PMOS as 2.5 times greater than that of the NMOS transistor. After performing this task, we need to size the transistors of each gate under worst case conditions (of input combination) for charging and discharging resistances Rc and Rd. (In every gate circuit, the PUN provides maximum ON resistance for rise time and the PDN provides maximum ON resistance for fall time.) For XOR and XNOR gates, worst case Rc/Rd ratio is equal to one. Therefore, (W/L)p must be equal to (2.5*1)(W/L)n for both gates.
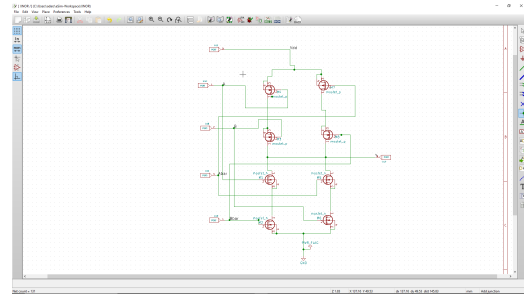
2 Implemented Circuit

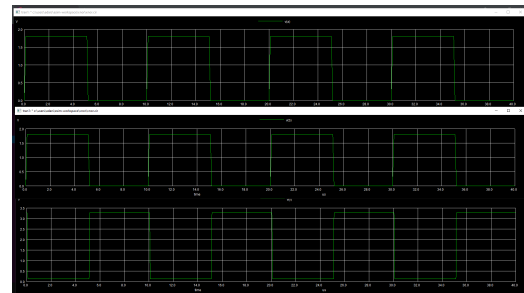Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] P. C. C. A. K. R. Aditi Joshi, Chanchal Jain. A comparative performance analysis of various cmos design techniques for xor and xnor circuits. www.ijraset.com ,Volume 5 Issue IV, April 2017 IC Value: 45.98 ISSN: 2321-9653.