Schmitt Trigger

DILIP BOIDYA, Tezpur University

July 28, 2021

Abstract

Schmitt trigger is an electronic circuit that transforms any analog and digital signal to noiseless digital signal it filters out any noise present in a signal line and produces clean digital signal. It is useful when noisy signals are involved. In this paper we will design CMOS logic based Schmitt Trigger Circuit & will generate its output waveform using eSim & sky130nm PDK, the main flaw in the comparator circuit is that, comparators aren't perfect if we observe the output voltage while monitored voltage crosses the reference voltage, then it can be seen that there's not one definite transition, there are even tons of pulses. To solve this and our noise related problems we will look towards Schmitt Trigger.

1 Circuit Details

CMOS Schmitt Trigger circuit has the switching thresholds are extensively dependent on the ratio of NMOS and PMOS. This circuit will exhibit racing phenomena after the transition starts. The three NMOS is loaded by the top PMOS circuit, the instant when output voltage Vout, is LOW, Third NMOS i.e., M5 will be OFF, hence the other two M1 and M2 NMOS run in triode mode of operation meaning the drain current is controlled by three terminals instead of two as in the saturation mode. When input voltage Vin to the terminal M1 and M2 is LOW, both the transistors operate in cut off mode. Hence both are in OFF condition. Transistors M3 and M4 are in ON condition that raise the output voltage to logic high level. When the input reaches the threshold voltage of the transistor M1, the M1 is turned on, while M2 is closed, then the high output turns on M5. Current starts to flow through M5. The node between M1and M2 is pull down by transistor M1. The on transistor M5 tries to pull up this node voltage. The transistor M2 is maintained at a high logic level output. When the input voltage exceeds the threshold M2, the output is switched to a low logic level. As a result the switching point is switched to a higher voltage, called VIH. When Vin falls from HIGH to LOW, PMOS shifts the switching point to VIL. The difference between the VIH and VIL is referred as HYSTERISIS voltage.

2 Implemented Circuit

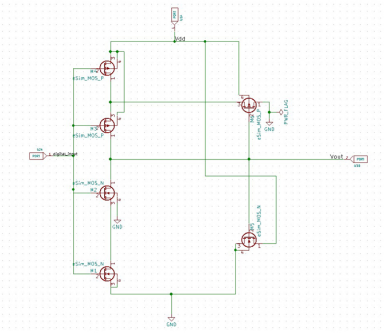

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

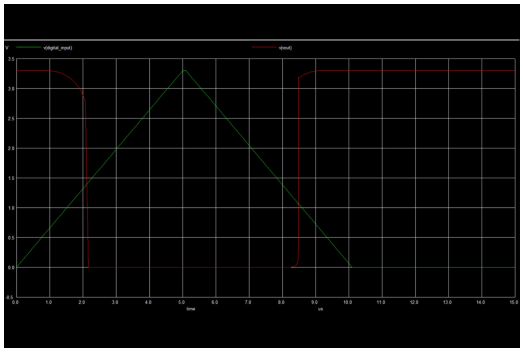

Figure 2: Implemented waveform.

References

[1] B. D. C. Chawla. A modified high hysteresis low power cmos schmitt trigger. https://www.ijraset.com/fileserve.php?FID=9839.

[2] M. Filanovsky and H. Bakes. Cmos schmitt trigger design. http://web.mit.edu/Magic/Public/papers/00260219.pdf.