Conversion of JK flip-flop to D flip-flop using CMOS-NOT Gate.

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Abstract

This is the implementation of Convertion of the JK flip flop to D flip flop,(for eSim Circuit design and simulation marathon conducted by FOSSEE IIT Bombay),involves in connecting the Data input (D) to the JK flip — flop through a combinational circuit and CMOS NOT gate for input to K from D. Here the Data input is connected directly to the J input and the inverted D input (using a CMOS NOT gate) is connected to K input .I used the application table of jk flip flop and the next state table of d flip flop derived from their functional table i was able to determine the values of j and k in terms of D. Circuit will be implemented on eSIM EDA tool and layout will be implemented using SkyWater130nm technology

1 Circuit Details

Convertion of the JKflip — flop to D flip — flop,involves in connecting the Data input (D) to the JK flip — flop through a combinational circuit and CMOS NOT gate for input to K from D. Here the Data input is connected directly to the J input and the inverted D input is connected to K input .I used the application table of jk flip flop and the next state table of d flip flop derived from their functional table and using k map i was able to determine the values of j and k in terms of D. Introduction to sequential circuits were made only because combinational circuits were not synchronous and output depends only on inputs which sometimes causes the output to reach unknown state. The flip-flops are sequential digital circuits whose outputs depends on input as well previous outputs and they are synchronous as well as asynchronous type. In VLSI flip-flops are recomended because of this property.D-ff is mostly used flip-flop.JK-ff is designed from basic SR-ff.This is the implementation of D-ff using JK-ff ,using next state table of D-flip-flop and application table of JK-ff .Comparing next state output of D-ff with application table of JK-ff and solving the K-map .We get the J =D and K=!D.After substituting the values of J and K in logic diagram of JK-ff we get the output of D-ff.When D=0,Qp=0,Qp(bar)=1,D=1,Qp=1,Qp(bar)=0. For CMOS NOT gate, PMOS and NMOS is used, when D is 0 PMOS is on and makes output 1 and when D is 1 NMOS is on and output becomes 0.Output from CMOS NOT is input to K.
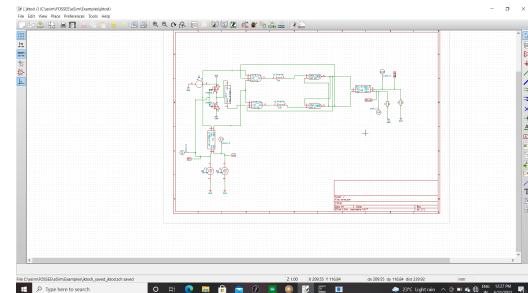
2 Implemented Circuit

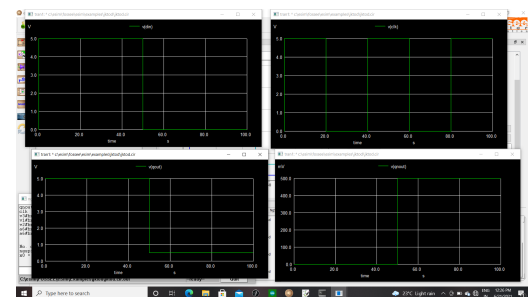Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] electronics hub. flip-flop conversion. www.electronicshub.org.

[2] john. flip-flop conversion->jk to d. www.CircuitsToday.com.