D Flip-Flop using CMOS

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Abstract

In this Project, the D Flipflop circuit has been implemented that is used in digital and analog systems. CMOS D Flipflop is widely used to implement different types of Binary Counter, Shift registers, analog, and digital circuit systems. Leakage power is the main significance of CMOS technology. The supply voltage to the given circuit should be reduced during the standby mode in order to reduce power dissipation and to develop the time of battery backup. The clocked transistors used in the implemented design are less which in turn reduces the dynamic power consumption as well as the leakage current.
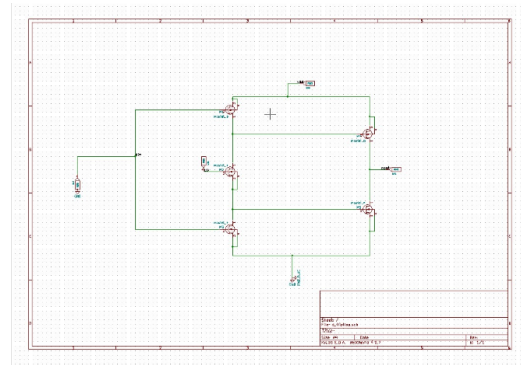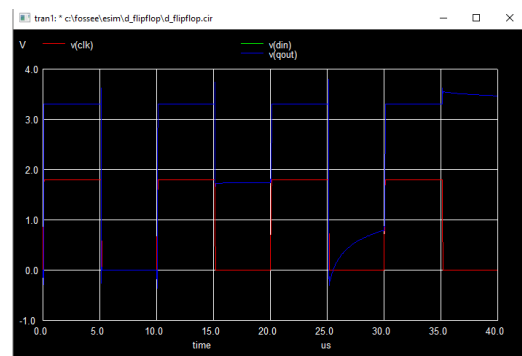
1 Circuit Details

The D flipflop follows the output which means that output will be the same as the input. D signifies " DATA" which means that it accumulates the value that is present on the data line. This D flipflop has been set or reset during the inverter circuit. Two types of flip-flops are single edge-triggered (SET) and double edge triggered (DET). Single edge triggered flipflop works on each increasing and falling edge of the clock which is easy to be implemented. The circuit that is implemented is the TSPC D flip-flop which has five transistors. The flip-flop is constructed using 3 NMOS and 2 PMOS transistors. Since the Edge triggered flip-flop has a low transistor count, therefore, it is small in the region and also decreases the power consumption. In 5 transistors TSPC D flip-flop, TSPC stands for True Single Phase Clocked logic. This circuit will be implemented using a single phase of the clock which avoids skew troubles. In the circuit implemented when the clock and the input D both are high, the transistors P1, N3 are OFF and the remaining transistors P2, N1, N2 are ON. Even in the ON clock period, the input is turned on as the output. When clock = 0 the circuit is in the standby mode and doesn't require more power to maintain in the standby mode. Hence even if we reduce the supply in standby mode it will work perfectly fine.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] M. Shakya and S. Agrawal. Design low power cmos d-flip flop using modified svl techniques. https://www.ijrar.org/papers/IJRAR1944229.pdf.