3_Stage_CMOS_Ring_Oscillator

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Abstract

The circuit in this paper is a Three staged Ring Oscillator, that contains 3 CMOS inverters and a dc power source of 1.8V. The technology node used in the circuit is 130nm. The delay time in each stage results in the Oscillation. Using the 130nm technology parameters we design this circuit. The circuit is simulated using the eSim software and the paper also includes the Circuit and Waveforms generated. Ring Oscillators usually contain only odd number of stages, ie. three or five or nine stages and so on. This Ring oscillator is mainly used in the design of Voltage Controlled Oscillators in Phase locked loops.

1 Circuit Details

Ring Oscillator circuit consists of 3 stages, with the presence of a feedback from the last stage to the first stage. The circuit consists of 3 CMOS inverters connected in a cascaded fashion, with the output of one connected to the next inverter. Each inverter consists of nMOS and pMOS transistor. In its basic form, the oscillation frequency mainly limited by the transit response of the pMOS transistor as the mobility of hole is two to three times lower than electron mobility in nMOS transistor. The MOSFETS used in the circuit are using the 130nm technology node. The required 130nm technology MOSFETS are acquired using the sky130_fd_pr, which consists of several models of MOSFETS, Diodes, Capacitors, Resistors etc. The circuit also has 3 capacitors which act as stray capacitance to filter out distortions in the Oscillations. Capacitor of 1 pico Farad is used. The dc source of 1.8V is used as the source voltage for the PMOS and NMOS. The plot generator is connected in the output of every stage. Transient analysis is performed from a time of 10us to 10.5us with a step of 10ns. The oscillations are achieved when the ring provides a phase shift of 2pi radians, thus each stage must provide pi/N delay, since N is equal to 3 in the circuit designed each stage provides a delay of pi/3 radians. The rest of the phase shift/delay of pi is provided by the dc inversion.

2 Implemented Circuit

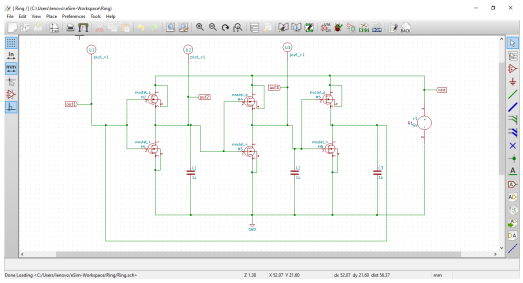

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

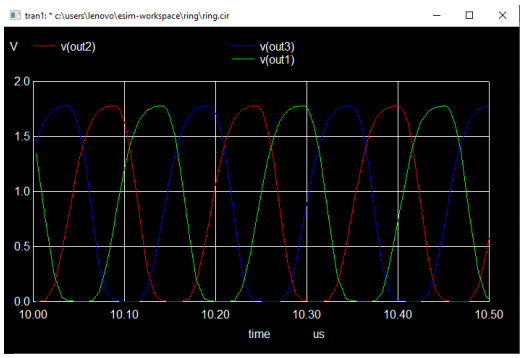

Figure 2: Implemented waveform.

References

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