NMOS Schmitt trigger SRAM

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Abstract

A SRAM with NMOS only Schmitt Trigger (ST) invertor with Voltage Booster (VB) circuit is presented. This is an efficient alternative to 6T SRAM because the CMOS based invertor is replaced by NMOS only ST to reduce the NBTI effect where only NMOS is used for both pull-up configuration also. The VTC of ST increases SNM ,a key FOM for SRAM and helps faster transition of output logic level for slow input transitions. Along with this, as compared to other SRAM configurations, the proposed circuit results lower dynamic power, delay, threshold voltage shift. The NBTI resilience, hysteresis loop VTC and higher SNM properties makes the proposed circuit a better alternative to 6T configuration.

1 Circuit Details

SRAM stores charge as long as it is powered. Unlike DRAM, it does not require refresh cycles, is faster albeit costlier due to higher gate density. The traditional 6T SRAM consisting of PMOS, poses critical performance degradation threat NBTI. It is observed in PMOS due crystal mismatches at the interface of metal and metal oxide interface and increases Vth (Threshold Voltage) of PMOS and reduces SNM resulting in reduced temporal performance, and potential device failure. The invertor proposed in the circuit has only NMOS. The VB boosts output of invertor from Vdd to Vdd1=Vdd+Vth (NMOS threshold voltage) to compensate the Vgs-Vth for M1 and M4 and pulls up Q and Q_ to Vdd during LH (Low to High) transition thus enhancing the swing of output voltage. The hysteresis VTC of ST reduces lower and raises higher threshold value for invertors, manifested as rise in SNM and faster transition as compared to 6T configuration. The circuit has 2 access transistors M9 and M10 controlled by WL (Word Line). There are 2 ST invertors who drive each other indefinitely as long as powered thus string the data. The invertors are connected to BL and BL (Bit Lines) for READ and WRITE operations through M9 and M10. The stored value is present at Q and complemented Q. To enable READ mode BL and BL are HIGH. After read destruction both BL and BL follow stored data Q and Q respectively and data stored is available at BL line. For WRITE mode, BL and BL are complementary. If new WRITE value is different to stored value, both invertors oppose the change initially and gradually change their states.

2 Implemented Circuit

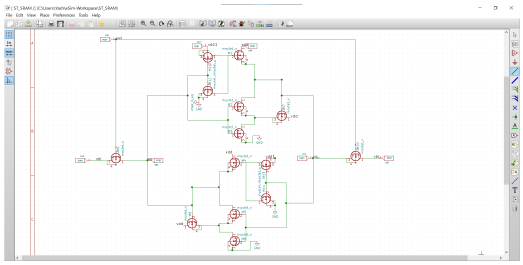

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

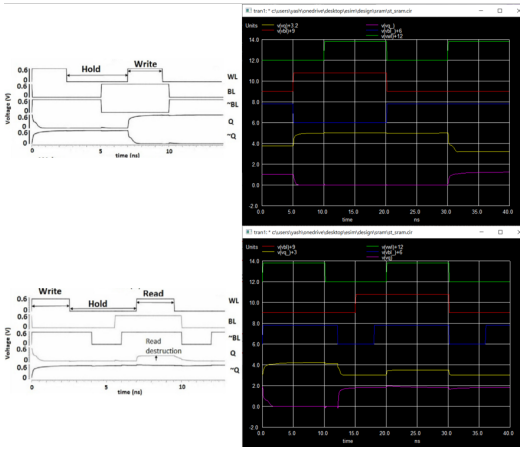

Figure 2: Implemented waveform.

References

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