Design of 4:1 Multiplexer using Transmission gates

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Abstract

The numerous analyses are primarily based on arithmetic circuits, particularly with MUX design, but this study also considers the use of a multiplexer to reduce power consumption. A novel 4 isto1 MUX is designed using CMOS Transmission Gate Logic , which reduces circuit complexity as compared to traditional CMOS based Multiplexer Designs. The proposed MUX Design removes the deteriorated output by combining the NMOS and PMOS for a strong output level with a gain in area, which is a primary outcome of the proposed MUX. Furthermore, it minimises the layout area.The design is also more efficient in terms of power consumption when compared to conventional design and can be used in ALU's.

1 Circuit Details

In comparison to a standard CMOS-based design, this design is a transmission gate kind of MUX structure with very few transistors. The transmission gate is a switch made up of back to back coupled PMOS and NMOS transistors. A strong 0 but a weak 1 is passed by NMOS devices, while a strong 1 but a weak 0 is passed by PMOS devices. By stacking NMOS in parallel with the PMOS device, the transmission gate combines the best of both features. A MUX structure is formed by connecting four transmission gates. Each transmission gate replaces the AND logic gate in a traditional MUX gate architecture by acting as an and switch. As a result, the number of devices is reduced. The transistor level architecture of 4isto1 MUX which consists of 44 transistors. The required functionality will consume more power with ample area due to an overabundance of transistors. However, as technology improves, the circuit should consume the least amount of electricity possible. As a result, this conventional design is not considered more advantageous for lower technology. So, this paper concentrated on transmission gate based 4:1 MUX design. Only 12 transistors are used in the proposed design. In the proposed design, the power consumption is decreased by using the smallest possible area.The transmission gate can be used to quickly isolate several signals with low signal degradation and little board area investment. A transmission gate is an electronic element that allows a signal level to be selectively blocked or passed from the input to the output.

2 Implemented Circuit

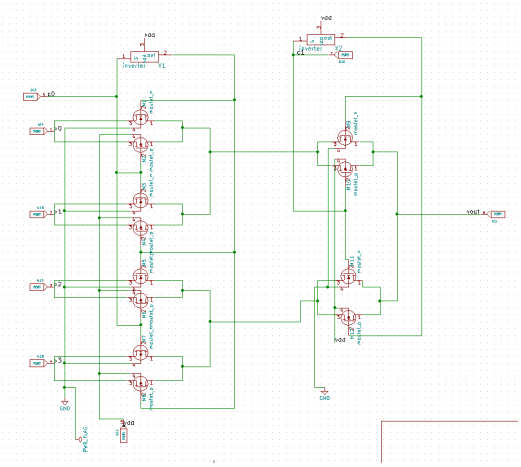

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

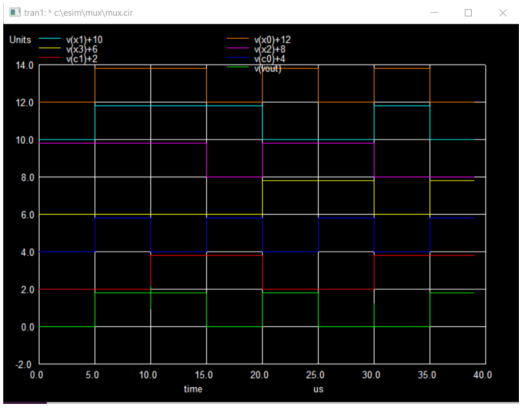

Figure 2: Implemented waveform.

References

[1] M.Mishra and shyam Akashe. High performance, low power 200 gb per sec 4isto1 mux with tgl in 45 nm technology. https://www.researchgate.net/publication/257799438.