FULL ADDER USING CMOS

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Abstract

The complexity in VLSI design increases with an increase in the level of integration. Full adder is designed using different low power techniques, such as, conventional CMOS, GDI, Modified GDI and hybrid full adders which has a combination of GDI, TG, XOR, XNOR and pass transistor logic. All the designs are compared for area, power and delay. Here CMOS technology is used for constructing various integrated circuits(IC) chips, including microprocessors, microcontrollers, memory chips and other digital logic circuits. Here I have implemented a conventional type of FULL ADDER using CMOS based on Skywater 130nm technology.

1 Circuit Details

The implementation of the FULL ADDER is done by using a sum of 28 MOSFETs of which 14 are NMOS and the other 14 are PMOS. The circuit takes in 3 inputs (A,B,C) and performs logical operations and gives out two outputs (SUM, CARRY).The dimensions of the mosfets are based on skywater 130nm pdk. The mosfet generally consist of three terminals namely source , gate and drain. For the transistor to conduct the applied gate to source voltage, Vgs must be greater than the threshold voltage, Vt. Only then a channel is formed and there will be a flow of charge in the transistor (electrons or holes) from source to drain. The gate terminal must be at positive potential with the source terminal for an NMOS to conduct and the gate must be at lower potential with source terminal in case of an PMOS . The circuit is provided with a Vdd of 3.3V and the digital inputs are of value 2.2V each (say A,B,C). The mosfets here acts like a switch whenever the digital input goes high at the gate, PMOS goes OFF and NMOS turns ON and vice versa. The inputs are delayed accordingly to match with the output waveform of the submitted file (literature survey) . Through this transistor operation the developed circuit performs logical operation of a full adder. The relations between the inputs and the outputs are expressed as: SUM = C(A+B+C)+ABC ,CARRY =AB+BC+CA.

2 Implemented Circuit

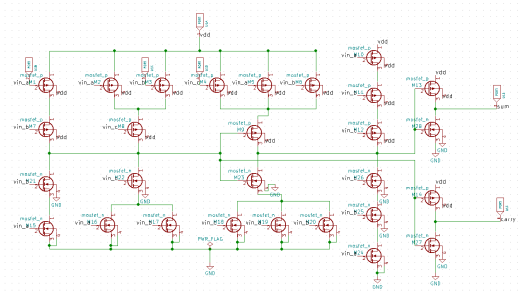

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

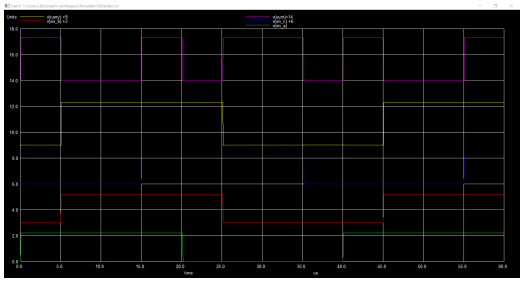

Figure 2: Implemented waveform.

References

[1] A. Chandrakasan. Low-power cmos digital design. https://ieeexplore.ieee.org/document/126534.

[2] K. Khare. Design a 1bit low power full adder using cadence tool. https://aip.scitation.org/doi/pdf/10.1063/1.3526237.