double edge pulse triggered JK flip flop

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Abstract

The clock provides a synchronized data flow which makes the technique useful in designing sequential net-works. Increase in the clock frequency and complexity of VLSI chips results in increase in power consumption. The major fraction of the total power consumption in highly synchronous systems, is due to the clock distribution. DET flipflops responds to both edges of the clock pulse offer potential advantages with respect to speed and power supply. Latches and flipflops makes the basic elements of clock system. Flipflop choice pro-vides better effect in reducing the power dissipation. DET JK flipflop is presented, which is designed directly based on characteristics of JK flipflops and pulse triggered flipflops.

1 Circuit Details

The implemented circuit is non inverting CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit. circuit consist of charge keeper circuit which is feedback controlled keeper circuit in order to combact the charge leakage and charge sharing that reduce the interval voltage during pre-charge mode and evaluation mode. As, we are implementing double edge pulse triggered JK flip flop pulses are needed to be generated both at rising edges and falling edges of a clock. The circuit is made up of two branches, one of which is in charge of implementing the transition from low to high level Q. The transition of Q from high to low level is implemented using the other branch. The delay metric for flipflops is minimum input data to output delay, which includes both setup time and clock to output delay. The Minimum delay time is obtained by sweeping the LOW-to-HIGH and HIGH-to-LOW data transition times with respect to the clock edge When the clock pulse is 1, J is 1 and K is 1,Q keeps the inverse of the previous state When the clock pulse is 1, J is 0 and K is 0,Q keeps the previous state When the clock pulse is 1, J is 0 and K is 1,Q is pulled down to 0. When the clock pulse is 1, J is 1 and K is 0, Q is pulled up to 1. When the clock pulse is 0, output Q and Qb keep the previous states.

2 Implemented Circuit

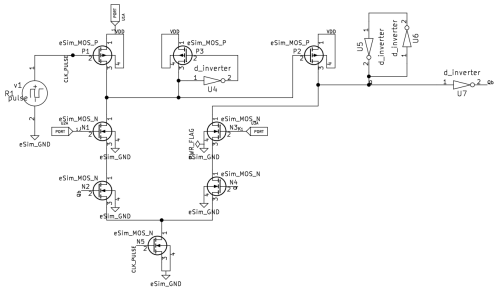

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

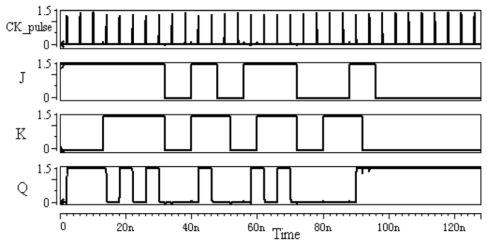

Figure 2: Implemented waveform.

References

[1] J. S. Y. Dai. An explicit pulsed double edge triggered jk flip flop. https://ieeexplore.ieee.org/document/5371580.

[2] J. P. Uyemura. Introduction to vlsi circuits and systems 2001, wiley. https://www.worldcat.org/title/introduction-to-vlsi-circuits-and-systems/oclc/714761912.