1-bit NP-CMOS Dynamic Full Adder

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Abstract

This circuit implements a single bit full adder using the dynamic NP CMOS logic style. This design is the result of an effort to implement a high speed, low power and low area 1 bit adder cell. Dynamic logic style is better than standard static mode in several factors like higher speed, rail to rail swing, non ratioed logic, no static power, and lesser no. of transistors. An N variable logic requires just N + 2 transistors compared to 2N transistors in static logic. NP CMOS specifically has advantages over other dynamic styles like Domino logic due to its scope for cascading. eSim tool was used for developing the schematic and running simulation. 130 nm CMOS technology from sky130 pdk was used for simulation.

1   Circuit Details
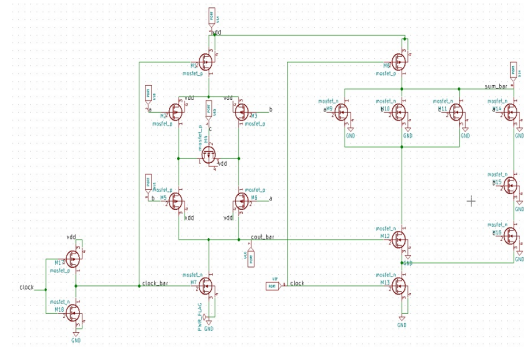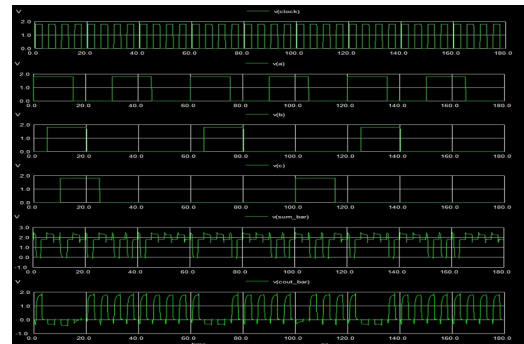
Full adder is an inevitable element in almost all digital system designs. So one of the major steps in improving the performance of a system is to develop a better performing adder model. Generally a full adder cell is a 3 input, 2 output block, where the inputs are ith bits of the operands and carry in from the previous block. Considering the research objective, the major drawbacks to tackle were to decrease the total number of transistors as standard CMOS logic required 2N transistors to implement an N input logic, to reduce power consumption as pseudo NMOS logic had static power loss due to its constant switched on pull up network, and to ensure rail to rail swing with high noise tolerance since pass transistor logic suffered from poor voltage levels and reduced noise margins. Dynamic logic, specifically NP CMOS offered the best alternative. Dynamic logic involves two phases, namely precharge and evaluation. Initially a single PMOS precharges the output node to Vdd at CLK = 0. A pull down network receiving inputs using NMOS implements the circuit logic during the evaluation phase, that is, when CLK = 1. In the first stage, (Cout)' is computed using bridge style. This output is used in the second stage to evaluate (Sum)' using, Sum = (Cout)' . (A + B + Cin) + A.B.Cin In total, 16 transistors are needed for the implementation. The inputs should be changed in precharge phase and the results are obtained during evaluation phase.

2   Implemented Circuit

Figure 1: Implemented circuit diagram.

3   Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] M. H. M. Keivan Navi, Reza Faghih Mirzaee. High speed np cmos and multi output dynamic full adder cells. https://www.researchgate.net/publication/290935969.