A Low Power 7T SRAM cell using Supply Feedback Technique CMOS

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Abstract

The downscaling of CMOS technology creates critical issues like power dissipation and stability in (SRAM). Which eventually degrades the performance of the SRAM cell. Hence to address the issue of data stability and power dissipation, this paper proposed a new (7T) SRAM cell to increases the write ability and reduces the static power consumption or dissipation using supply feedback transistor. Whereas the HSNM, read delay, and static power consumption or dissipation of proposed 7T is decreased by 1.08x, 1.3x, and 1.5x respectively in comparison to basic 6T SRAM cell at the same power supply. The newly designed 7T SRAM cell has been calibrated in the Esim and sky130.

1 Circuit Details

This project proposes a novel 7T SRAM cell. In the proposed design the read and write operation have been performed separately using read and write port to enhance the data stability. Furthermore, the supply feedback transistor has been used between data storing node and cell power supply in order to increase the write ability of the SRAM cell. .The main aim of this 7T SRAM cell is to reduce the consumption of leakage power and improve the stability of the memory cell in normal region of operation. Some design architecture used CMOS transistor operation in subthreshold region for reducing power. A modified 8-T design architecture is proposed for low power and low voltage circuits. The proposed 7T SRAM cell using supply feedback concept, which comprises of 4 NMOS transistors and three PMOS transistors. Transistor PM1, PM2, NM1, and NM2 forms the latch of SRAM cell where the data has been stored, whereas NM3 acts as an access transistor during the write operation which is activated by word line (WL) signal and NM4 acts as an access transistor during read mode which basically used to separate the RBL from storing nodes Qb and Q of SRAM cell for providing disturb free read operation. The transistor PM3 acts as a feedback transistor which is connected between the power supply and storing node Q. When feedback transistor PM3 is ON state, the voltage at the drain of PM3 is slightly lower than the supply voltage. The bitline (BL) is an input line of a cell during write operation whereas RBL is input or output line during the read operation.

2 Implemented Circuit

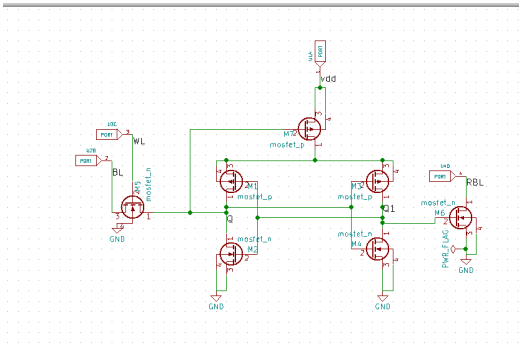

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

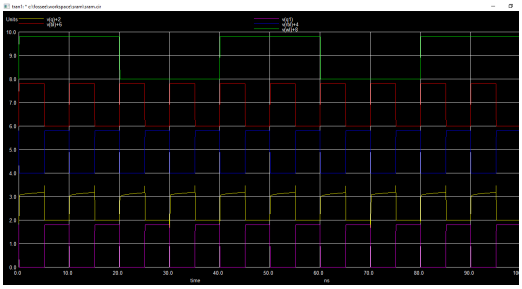

Figure 2: Implemented waveform.

References

[1] J. K. M. P. K. M. M. Goswami. A low power 7t sram cell using supply feedback technique at 28nm cmos technology. https://ieeexplore.ieee.org/document/9071308.