AND gate using CMOS technology

B ABHISHEK, KLE technological university, HUBLI

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Abstract

In this page, 2 bit AND gate is implemented using MOSFET device based on 130nm technology using skywater130nm process design kit. This circuit is designed in ESIM simulator and simulated using ngspice simulator. AND gate is used in various digital circuit applications. To understand the nature of the digital AND gate truth table is necessary so, by providing the input waveforms according to the truth table the output is recorded by representing the output waveform. AND gate is performed by using NAND gate and inverter where, NAND and inverter are designed using PMOS and NMOS. Using PMOS and NMOS the performance of the AND gate will be enhanced.

1 Circuit Details

The circuit details are given here, The two input AND gate designed using 3 PMOS and 3 NMOS, where firstly by designing two input NAND gate using MOS requires two PMOS and 2 NMOS. Vdd of 5 volts is provided to drive the current through MOSFETS and grounding the circuit to provide NMOS operations. Input Va and input Vb is given to the two input NAND gate and the output of the NAND gate is given as the input to the next module which is inverter. Inverter takes the output of the NAND gate and provides the inverted value in this case the inputs are given in binary format 0,1 as waveforms or pulse . The inverter is designed by using a PMOS and an NMOS which also represents the functionality of CMOS i.e complimentary MOSFET name itself says the voltage gets complimented, the same operation is used in designing 2bit AND gate. The final output of the design is represented by the waveform. Once the circuit is designed in the esim simulator MOSFETS should be converted to the 130nm technology using sky130pdk libraries. Two inputs Va and Vb pulse is given to the circuit and the output is recorded as Vout waveform the simulation is done after converting mosfets into 130nm technology by creating the spice netlist and representing in sky130nm format and the simulation is done using the ngspice . The final output shows the characteristics of AND gate that is vout is high only when bothe Va and Vbare high , low otherwise. The design is represented as shown .

2 Implemented Circuit

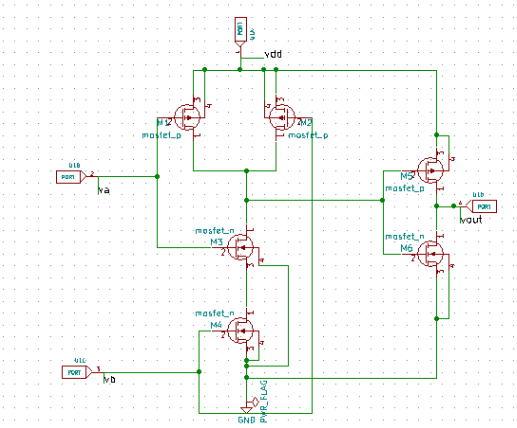

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

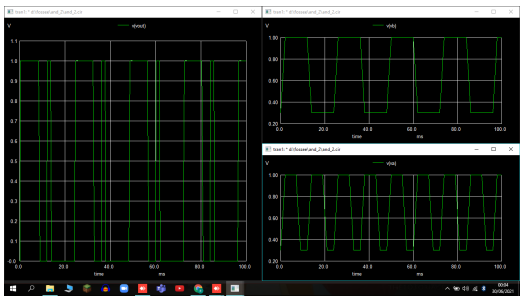

Figure 2: Implemented waveform.

References

[1] Sidhartha. Nand and nor gate using cmos technology. http://www.vlsifacts.com/nand-gate-using-cmos-technology/.