

D Latch using CMOS Transmission Gate(TG) switches

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Abstract

This paper introduces the design of a low power CMOS D latch using two transmission gates and two inverters. A D latch is an electronic device that can store one bit of data. The D latch captures the logic level of the Data line whenever the enable signal is high and latches the last logic state whenever the enable signal is low. The main advantage of the CMOS implementation of the D latch is that it consumes very low power when held in a static state and it also reduces the complexity of the circuit to some extent. The proposed circuit is implemented in the Esim EDA and is adjusted with the Sky130 PDK. After that the output Q and Q1 are analysed for the given input Data and Enable line.

2 Implemented Circuit

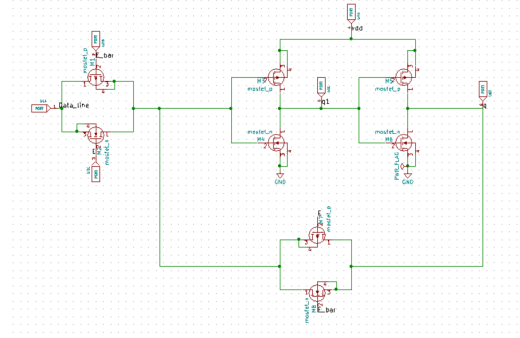


Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

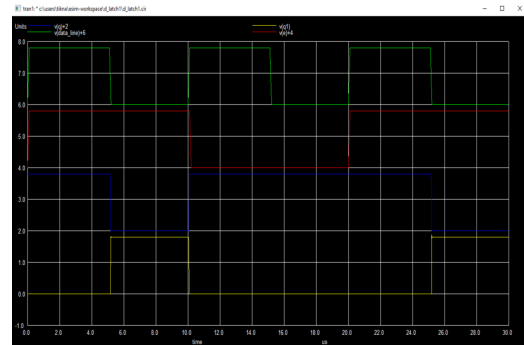


Figure 2: Implemented waveform.

1 Circuit Details

D latch is a 1-bit memory device having only one input and an enable signal. When the enable signal is 'High' the latch will be responsive and the Data line will be same as input the input is high. When the enable signal is 'Low', the last input of the D latch will be latched on and it will not be responsive to the input Data line. In this design of the D latch in Esim, two transmission gates and two inverters are used. There is one transmission gate where the input is given. When enable is High the transmission gate will be turned on. This transmission gate will give us the output same as input when enable signal is High. This is the Q output of the latch. The Q output is the fed into two inverters which is connected to another transmission gate which connects to output of first transmission gate. The output from the first inverter is the Q1 output. In the circuit, the Enable signal is provided to the NMOS and Enable bar is provided to the PMOS of the first transmission gate and vice versa in the second transmission gate. So, the first transmission gate operates in Enable High and the second in Enable Low. As a whole the first transmission gate provides the present output when enable signal is high and the two inverters along with the other transmission gate provides the latched output when enable is low. This is the circuit that is implemented and simulated in this paper. The screenshot of the circuit designed in Esim along with screenshot of the input and output waveforms simulated in Ngspice using sky130 PDK are attached below.

References

- [1] G. Scotti. Design of low-voltage high-speed cml d-latches in nanometer cmos technologies. <https://ieeexplore.ieee.org/document/8048001>.