2:1 Multiplexer using CMOS logic

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Abstract

A multiplexer is a unidirectional device which is used in any application in which data must be switched from multiple sources to a destination. It is a combinational circuit which has a maximum of 2 to the power n data inputs, 'n' selection lines and a single output line. One of these data inputs will be connected to the output based on the values of the selection lines. Multiplexers are used in building digital semiconductors such as CPUs and graphics controller, as programmable logic devices, in computer networks and digital video. This paper presents a 2:1 multiplexer using CMOS logic. The implementation is done in VLSI technology as it has features like small size, low cost, high operating speed and low power.

1 Circuit Details

A 2 to 1 multiplexer consists of two inputs 'vin1' and 'vin2', one select input 'select' and one output 'vout'. Depending on the select signal, the output is connected to either of the inputs. Since there are two input signals, only two ways are possible to connect the inputs to the outputs, so one select signal is needed to do these operations. Ignoring the don't care conditions, we can derive the Boolean Expression of a 2 to 1 Multiplexer as vout= selectbar(vin1) + select(vin2), where selectbar indicates negation of select signal. The static CMOS based 2:1 MUX using the above Boolean expression has been designed using a pull-up network consisting of 4 pMOS and a pull-down network consisting of 4 nMOS. The pull up network is constructed using two parallel pMOS circuits connected in series. The pull-down network is constructed using two series nMOS circuits connected in parallel. The output of the Static CMOS logic is connected to an inverter to obtain the correct output. VDD is connected to the pull-up circuit to provide power supply and the ground is connected to the pull-down circuit. The input vin1 is a pulse wave of width 5us and input B is a pulse wave of width 2.5us. One of these inputs is selected based on the select signal pulse. One of the major advantages of Static CMOS logic is that they have zero quiescent power dissipation, where for any applied input state either the pull-up network or the pull-down network remains off. The problem with this type of implementation is that more area is required in implementing logics.

2 Implemented Circuit

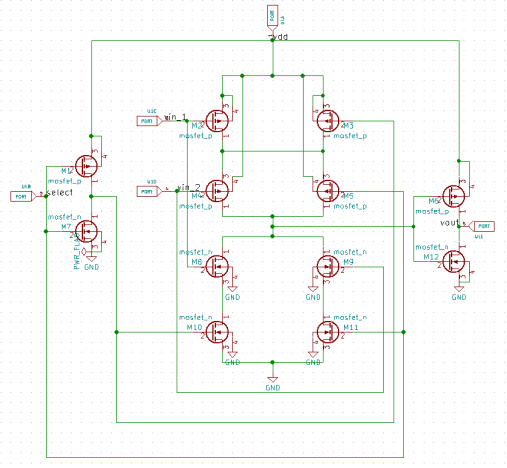

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

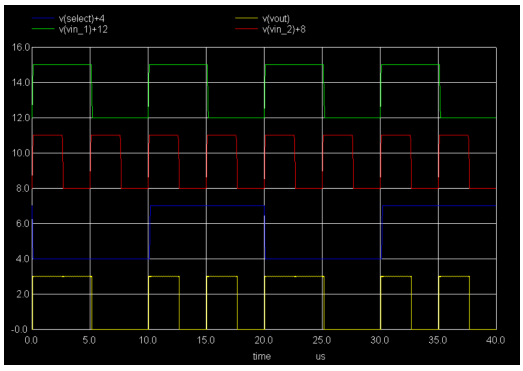

Figure 2: Implemented waveform.

References

[1] T. Dua. 2:1 multiplexer using different design styles: Comparative analysis. https://www.researchgate.net/publication/349211497_21_Multiplexer

[2] K. Sharma. Low power and high speed 2:1 mux various cmos logic using svl technique. https://www.ijrar.org/papers/IJRAR1944227.pdf.