Full Adder implementation on Dynamic CMOS Logic

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Abstract

Complementary metal oxide semiconductors(CMOS) technology is a technology used to Build Integrated circuits chips. CMOS Technology has advantages such as Very low static power consumption, Reduced Complexity of the circuit, Pure logic 1 or 0 output and Resistance to high level of electronic noise. Our design is based on designing Full adder using CMOS logic. As Full adder is One of the main operations involved in many higher Hierarchal operations. Thus improving the its efficeincy will directly improve the overall efficiency of the circuit. We use the PMOS and NMOS for implementation and to obtain the proposed circuit. The simulation and Waveform generation part is completed through Esim simulator and Ngspice.

1 Circuit Details

The circuit is implemented using the using CMOS logic (combination of MOSFETS(i.e.NMOS and PMOS)) . The Full adder circuit Has two output (i.e. Sum output and Carry ouput). At first, The circuit. Equations are reduced for implementing the circuitry. The circuit totally consists of 40 mosfets considering both Sum and carry circuit. As CMOS logic gives an inverted output an Inverter is used For realising the Actual output. The inputs to the circuit Are A, B, cin. A1, B1, cin1. Here A1, B1 and cin1 are the inverted values of input A, B and cin respectively Which are used While realising The Ouput of Sum Circuit. The equation realised for obtaining Sum output is A1(B1cin+Bcin1) + A(B1cin1+Bcin). Similarly the equation realised for obtaining Carry output is cin(A+B)+AB. The Complete circuit simulation is done Through esim simulator Where Annotations check,Electrically rule check and Netlist generation Tasks are proceeded. The Output of Simulation(Netlist) is mapped with Librabries of Skywater 130nm PDK . Here Skywater 130nm technology is a mature 180nm-130nm hybrid technology Developed by Cypress semiconductors and Later Collabarated with Google which is open sourced for industry usage . The Output Waveforms for the Designed circuitry with Generated Netlist Mapped with SKY130 nm Libraries are checked using Ngspice (Which is also a open Source Spice simulator Tool). Thus the output waveform is Then checked for correctness and functionality For the implementation of Full adder circuit..

2 Implemented Circuit

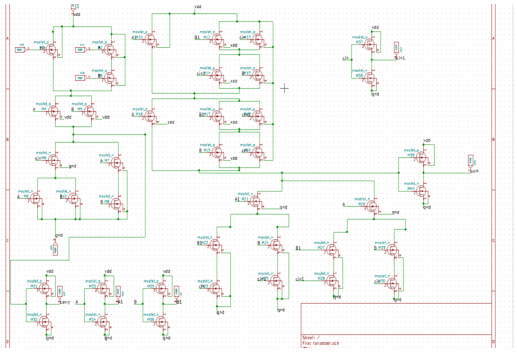

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] S. K. A. B. Shamim Akhter, Saurabh Chaturvedi. An efficient cmos dynamic logic-based full adder. https://ieeexplore.ieee.org/document/9182729.