Full Adder using CMOS

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Abstract

The project aims to design a full adder circuit using CMOS. A full adder is used to add three 1-bit numbers to give a sum output and a carry output. It overcomes the limits of a half adder that can add only two 1-bit numbers, as it also incorporates the carry of the previous addition. Full adders can be used as part of many other larger circuits like Ripple Carry Adder, which adds n-bits simultaneously. They are also used in Arithmetic Logic Unit/ALU. The use of CMOS in IC design has seen a tremendous upsurge over the past two decades. This can be attributed to the many advantages they provide, like extremely low consumption of static power and the ability to integrate a large number of components on small chips.

1 Circuit Details

The full adder circuit has 3 inputs – A, B and Cin. It has 2 outputs – Sum and Cout, and thus there are 2 sets of pull-up and pull-down networks. As we know, the pull-up network consists of pMOS and the pull-down network consists of nMOS transistors. In the circuit for the Carry output, there are 5 of both pMOS and nMOS transistors. Now, we know that the equation for the Sum output is conventionally given by (A exor B exor C). But, this gives rise to complications in designing the circuit as there would be a lot of transistors, and the circuit would be very expansive. Thus, we go for an alternative path and take the Cout bar output and feed it into the Sum circuit as the 3rd input. This eases the equation for the Sum output by expressing it in terms of A, B, Cin and Cout, rather than exor operations. It also reduces the number of CMOS transistors required in the Sum circuit and hence the overall design. We obtain the required number of both pMOS and nMOS as 7 for the Sum. Also, since CMOS circuits always provide an inverted output, we need to add inverter circuits to both the Sum and Cout outputs to acquire the originally required outputs - hence costing us 2 more of both pMOS and nMOS for each output inverter. The number of CMOS transistors used thus comes to a total of 28. NOTE : The waveform obtained although correct and in accordance with the truth table of Full Adder, does not exactly resemble the reference waveform provided in the literature survey report.

2 Implemented Circuit

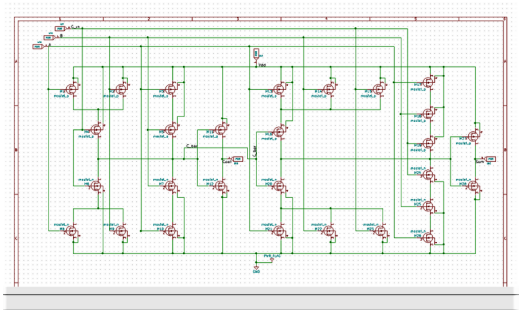

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

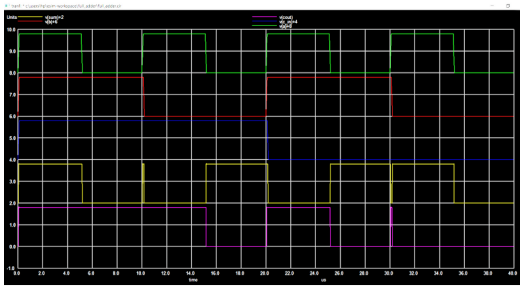

Figure 2: Implemented waveform.

References

[1] V. Rajeswari. Adder – classifications, construction, how it works and applications. https://electricalfundablog.com/adderclassifications-construction/.