3T NAND gate

Akhil Hadli, BMS College of Engineering

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Abstract

This paper proposes a new design for a two input NAND gate which uses 3T to implement 2 input NAND gate. This design is superior in terms of speed and power compared to other available structure. The proposed 3T NAND gate effectively outperforms the basic CMOS NAND gate with excellent driving capability and signal integrity with exact output logic levels. The proposed robust three transistors 3T based NAND gate is just as effective for dynamic power control in CMOS VLSI circuits for System on Chip SoC applications. The 3T NAND gate lead to better performance measures in terms of reduced area and high speed while maintaining comparable performance than the other available NAND gate logic structures.

1 Circuit Details

The 3T NAND Gate function is as follows. The PMOS M1 and NMOS M2 on the left form a modified CMOS inverter structure. The PMOS M3 on the right acts as a pass transistor. When A is 1 M3 is OFF and the modified inverter on the left M1 and M2 functions as a normal CMOS inverter. The output is the complement of input B. When A is 0 and B is 0 M2 is OFF M1 and M3 are ON which leads to an undefined output state X. Because M1 tends to pull down the output node while M3 tends to pull up the output node. Similarly when B is 1 M1 is OFF M2 and M3 are ON leading to an undefined output state X .Because M2 tends to pull down the output node while M3 tends to pull up the output node. Similarly when A is 0 B is 1 M1 is OFF M2 and M3 are ON leading to an undefined output state X .Because M2 tends to pull down the output node while M3 tends to pull up the output node. For A is 0 and B is 0 or 1 and a strong logic 1 output is required. It is possible to obtain exact output logic levels with the proposed circuit, if the channel width of M3 is made 6 times that of M2 or 3 times that of M1.Thus M3 becomes much stronger than M1 and M2giving a strong logic 1 at output when input A is 0.The proposed 3T NAND gate is exempted from body bias effect as there is no stacking of transistors. Good output logic levels are attained for all the input combinations with some voltage degradation in sky130 pdk . Good output logic levels are attained for all the input combinations without any voltage degradation
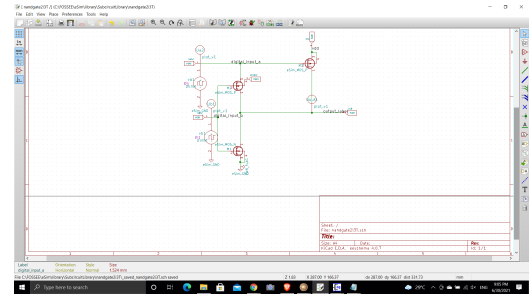
2 Implemented Circuit

Figure 1: Implemented circuit diagram.
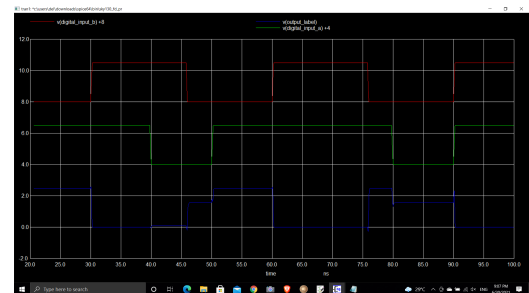
3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] M. G. Priya and K. Baskaran. A novel low power 3 transistor based universal gate for vlsi applications. https://www.researchgate.net/publication/290348200_A_Novel_Low_

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