SR Flip Flop using CMOS Technology

Manjit Kalita, Assan Engineering College

July 1, 2021

Abstract

This paper presents a SR flip flop designed using CMOS technology. A flip-flop or latch is a circuit that has two stable states and can be used to store state information-a bistable multi-vibrator. Flip flop has a control signal or clock signal which is a time varying voltage signal applied to control the operation of a flip flop and has equal time duration of High Pulse and Low Pulse. The circuit uses CMOS transistors providing low power consumptions with a large fan out capability. The circuit produces output set, reset and hold state. The proposed SR flip flop will be implement in eSim using the Sky 130 PDK. After that, we will analyze the output set, reset and memory values of the flip flop.

1 Circuit Details

The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labelled as S and R, respectively. The reset input is used to get back the flip flop to its original state from the current state with an output Q. This output depends on the set and reset conditions, which is either at the logic level 0 or 1. The circuit can be made to change its state by applying signals to one or more control inputs and will have one or two outputs. Flip flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited period of time sufficient for other circuits within a system to further process data. The CMOS circuit will have two pull up networks and two pull down networks. The first PUN has 3 PMOS connected with the 3 NMOS of the PDN. This gives the output Q'. Similarly, another two same PUN and PDN are connected to get output Q. Now the output Q' is connected with inputs of second PUN and PDN, and output Q with inputs of first PUN and PDN. The low i.e. GND and high i.e. VDD that are supplied are used as binary 0 and 1. This CMOS circuit will be made to get our required SR flip flop.

2 Implemented Circuit

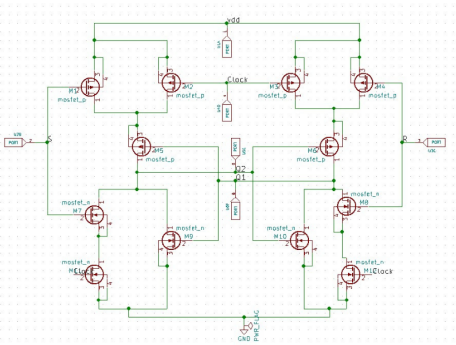

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

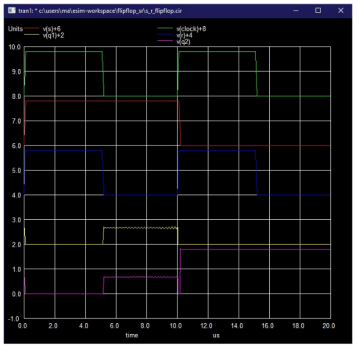

Figure 2: Implemented waveform.

References

[1] A. Kaur. Layout design analysis of sr flip flop using cmos technology. https://dokumen.tips/download/link/layout-design-analysis-of-sr-flip-flop-using-cmos-technology.