2x1mux using CMOS

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Abstract

I am going to implement 2x1 mux circuit using Complementary metal oxide semiconductor or CMOS technology and also I will implement it by using sky130nm technology using esim and ng spice simulation software. Multiplexer are those devices converting 2n number of inputs into one single output. In the 2n number n stands for the select pin which determines and decides that which pin will input first and which pin will input later. The meaning of 2x1 multiplexer is that it is designed in such a way so that they can acknowledge and decide amongst the two pins which pin will reach the output first. And using CMOS it will also consumes less power ,lower propagation delay than NMOS, very high noise immunity and noise margin.

1 Circuit Details

Multiplexer is sometimes known as a data selector. A 2x1 multiplexer having two inputs A and B one selection input S and one output line Y. As we can see there does one prefer inputs therefore, they can have only two achievable combinations starting from 0and 1. When selection input is 0 then input line A is preferred and is directed to the output. Similarly when selection input is 1 then input line B is preferred and is directed to the output Y for their combination of these selection inputs. Here we consider a 2x1 multiplexer with inputs as A and B with select inputs S and Sbar and output Y. Circuit operates as when select line S is in Logic low and Sbar is in logic high then output selects A and passes the supply voltage to output Y. Or else when select line S is in logic high and Sbar is in logic low then output selects B and passes the supply voltage to the output. As we know the equation of the 2x1 multiplexer is Y=ASbar+ BS. So according to the CMOS design rules the pull up network should be made of PMOS transistors and connected to VDD and pulldown network should be made of NMOS and connected to GND. So according to rules for getting ASbar and BS all the 2 PMOS pairs should be connected in parallel and then two parallel connections should be added in series. For pull down network 2 NMOS pairs should be connected in series for getting ASbar and BS then two series connections should be added in parallel. We all know that the output of a CMOS circuit is inverted so to get the actual output we must add a CMOS inverter. And we will simulate it on sky130 nm technology.

2 Implemented Circuit

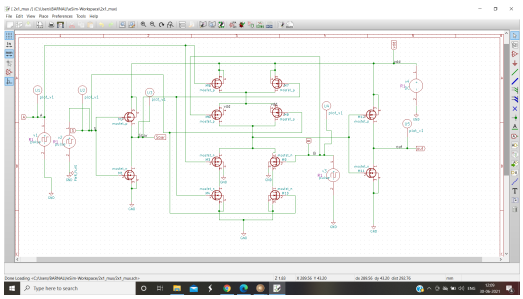

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

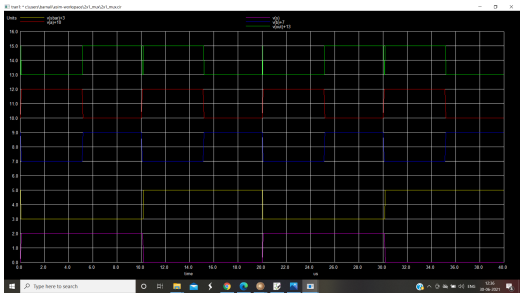

Figure 2: Implemented waveform.

References

[1] S. J. Anjum Aara. Design and implementation of cmos and cnt based 2x1 multiplexer at 32nm technology. https://www.irjet.net/archives/V6/i8/IRJET-V6I895.pdf.

[2] P. P. V. R. M.PAVAN KUMAR, V.SASIKALA. An efficient level converter model for power optimization. http://www.ijvdcs.org/uploads/532641IJVDCS16642-48.pdf.

[3] Y. L. Sung-Mo Kang. Cmos digital integrated circuit. https://digitalsystemdesign.in/wp-content/uploads/2018/05/C-MOSkang.pdf.