Current mode logic CML latch

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Abstract

An conventional current mode logic CML latch is proposed in this paper. The latch uses an NMOS transistor controlled by clock signal to improve the tail current I of the latching branch, so as to improve the speed of the latch. Implementation of the circuit is done using SKY 130nm technology. To operate at very low bias current I, a simple and compact high resistance load R has been introduced. CML circuits are used to gain higher speed in high frequency applications. Especially CML latches are widely used in many high speed applications, such as multiplexers and demultiplexers, clock recovery circuit and so on. and data recovery circuits, frequency dividers, and so on.

1 Circuit Details

CML latch has the two sub parts: CML buffer and regenerative latch. The basic CML buffer is the simple differential amplifier with two resistor loads value R. Both transistor should be in saturation. The transistor which is closest to getting into triode is the one whose input is at VDD which can be treat as boundary condition. Hence, we must choose the logic swing Io into R to be less than threshold volatge of transistors. A regenerative latch in CML logic can be implemented by connecting the output to the input of CML buffer to get the positive feedback. For regeneration and latching, we need gm greater than 1/R. The input clocks of CML buffer and regenerative latch are complemented. To make sure all transistors are in saturation we must use appropriate common mode voltage. When clock is low, the second stage with positive feedback is disabled, and the circuit is a simple differential amplifier. This is the phase when the output tracks the input with some gain. When the clock goes high, the input amplifier stage is disabled, and the regenerative second stage is activated. The second stage then regenerates from where the amplification stage left the outputs and produces a logic output depending on the sign of the initial voltage. The designed circuit is only a latch. To make a flip flop that samples on every clock edge we need to use two latches in a master slave fashion.

2 Implemented Circuit

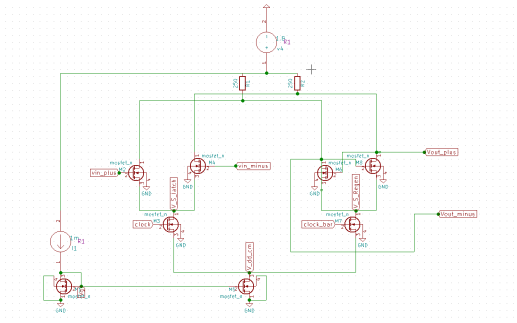

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

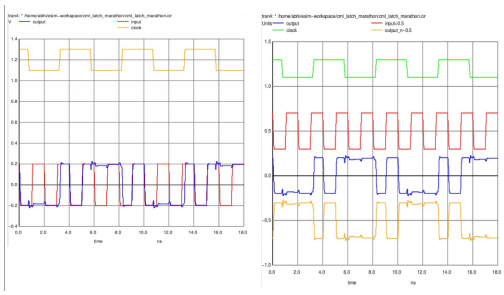

Figure 2: Implemented waveform.

References

[1] P. Heydari. high-speed cmos cml buffers and latches. https://ieeexplore.ieee.org/document/1205938.

[2] M. k. Santosh Kumar Vishvakarma. An improved current mode logic latch for high-speed applications. https://onlinelibrary.wiley.com/doi/abs/10.1002/dac.4118.