NAND Gate using CMOS in 130nm technology performed in e-sim

Vanshika Tanwar, Dronacharya Group Of Institutions

October 15, 2021

Abstract

Logic gates are the building blocks of any circuit. There are different types of logic gates like AND, NAND, etc. When we internally implement all these logic gates using transistor and diodes then it comes under logic families. So, in this paper we are going to do the analysis of NAND GATE using CMOS in SKY130nm Technology. We are implementing NAND GATE using CMOS because CMOS become very much useful in VLSI industry. The entire design of NAND GATE has been performed using SKY130nm Technology. We are going to carried out the whole simulation of the proposed design of NAND Gate in esim Software which is an EDA tool. And by changing the different values of inputs of NAND Gate we are observing respective output.

1 Circuit Details

For implementation of NAND Gate using CMOS, we connect Both PMOS in parallel with each other and NMOS in series with each other. Let us take PMOS as M1 and M2 and NMOS as M3 and M4, Vcc1(high voltage) and GND(Ground). There are two input Ain and Bin in NAND Gate. 1)When Low input is given to both Ain and Bin input of NMOS and PMOS then both M1 and M2 comes in ON state and become short circuited. Also, Both M3 and M4 comes in OFF state and become open circuited. It gives Vcc1 at output Yout(high). 2)When Low input is given to Ain and High input is given to Bin of NMOS and PMOS, M1 comes in ON state and it become short circuited and M3 comes in OFF state and it become open circuited. Now comes to input Bin which goes into M2 and M4.M2 comes in OFF state and it becomes open circuited and M4 comes in ON state and it become short circuited. Also, When High input is given to Ain and Low input is given to Bin of both NMOS and PMOS, as High input is given in Ain, M1 comes in OFF state and it becomes open circuited and M3 comes in ON state and it becomes short circuited. Now comes to input Bin which goes into M2 and M4.M2 comes in ON state and it become short circuited and M4 comes in OFF state and it becomes open circuited. So, output of both comes at Yout is Vcc1(high). 3)When High input is given to both Ain and Bin input of NMOS and PMOS, both M1 and M2 comes in OFF state and both becomes open circuited. Also, at the same time Both M3 and M4 comes in ON state and both becomes short circuited. As, M3 and M4 becomes short circuited then it gives GND at output Yout(low).
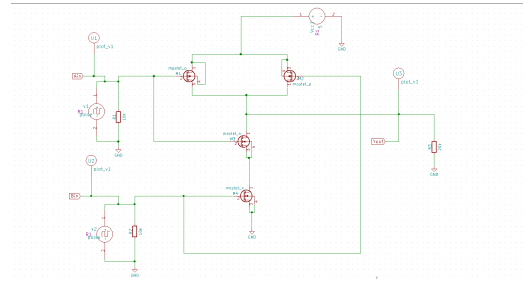
2 Implemented Circuit

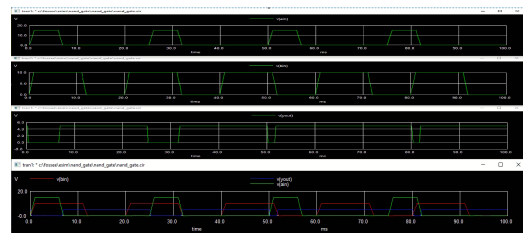Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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