Design of 2 bit Parity Generator using Pseudo NMOS logic

Mahisha.B.M, R.M.K.Engineering College

July 1, 2021

Abstract

Parity generator is a combination logic circuit. When data is transmitted between source and destination there should not be any loss in data. To prevent data loss parity generator technique should be used in transmitter end. Parity is the extra bit added to digital data on transmission. There are two types of parity generator even parity generator and odd parity generator.Even parity generator look for even number of ones in binary data here parity bit is one for odd number of ones else it is zero.Odd parity look for odd number of ones in binary data here parity bit is one for even number of ones else zero.Two XOR gates are used to implement parity generator. XOR gate is constructed using pseudo NMOS logic. .

1 Circuit Details

A 2 bit even and odd parity generator is constructed by cascading 2 Exclusive OR or XOR gates. XOR is a gate which gets 2 inputs and leaves an output. In XOR gate output will be true or high only when there is an odd number of one is given as input and output will be false or zero when even number of one is given as input. XOR gate is implemented using pseudo NMOS logic. Pseudo NMOS logic is a type of static cmos logic where complementary output is driven between Vdd and ground. This complementary output can be normalized by cascading an inverter to it. In this logic the number of transistors required is N plus 1 where N is the number of inputs. A complete logical expression is implemented using NMOS transistors with one PMOS transistor which is grounded . vdd is given to the source terminal in pmos. In this design we have taken two inputs A and B with one output PARITY BIT. T he type of parity generator is choosen by baising Dc source at pin 5 and pin 7. If DCunderscoreB is high odd parity is generated. If DCunderscoreB is low then even parity is generated. Odd parity denotes ODD PARITY BIT and even parity denotes EVEN PARITY BIT. Expression for ODD PARITY BIT is equal to A XNOR B. Expression for EVEN PARITY BIT is equal to A XOR B. Pin 1 is A Pin 2 is D which is B bar pin 3 is C which is Abar pin 4 is B pin 5 is DCunderscoreD pin 6 is vdd pin 7 is DCunderscoreB and pin 8 is PARITY BIT. We can get output plot from 8th pin.

2 Implemented Circuit

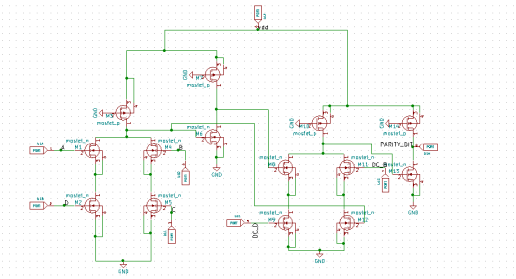

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

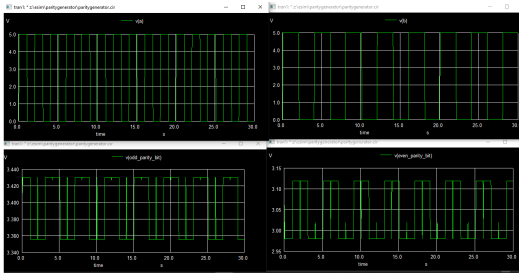

Figure 2: Implemented waveform.

References

[1] W. Musa. Design of digital parity generator layout using 0.7. https://www.researchgate.net/publication/328020132.