CMOS Rail-to-Rail Operational Amplifier

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July 1, 2021

Abstract

This paper presents the design and analysis of an operational amplifier with rail-to-rail input and output capability. The study characterizes the rail-to-rail input and output stages to formulate a standard design approach that can be used as a reference for future projects and researches in the area of rail-to-rail amplifiers. The design is achieved using complementary differential pair with cascode load as the input stage, and push-pull inverter as the output stage. The op-amp is implemented using CMOS technology, and the simulation results are equivalent to commercially available circuits in terms of offset voltages, gain, and common mode rejection ratio.
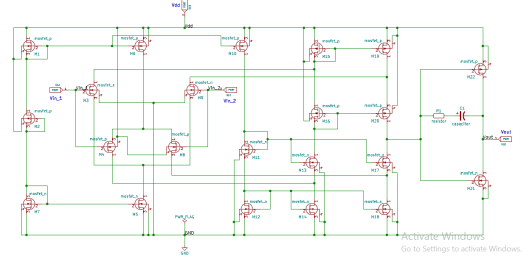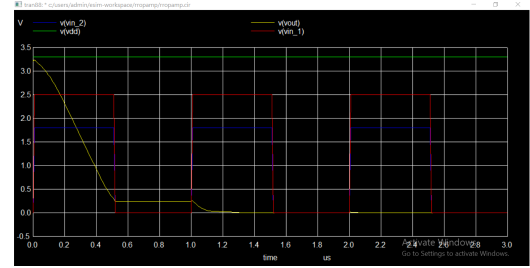
1 Circuit Details

Rail-to-rail op-amps allow signals to swing from negative supply rail to the positive supply rail. Nowadays, rail-to-rail operational anplifiers play a significant role in various biomedical applications. Earlier rail-to-rail op-amps were designed using BJTs, now CMOS technology is utilized. CMOS transistors have an edge over BJT in terms of very high input impedance, high speed, and low leakage current. The topology of the input stage is based on the folded cascade op-amp with a PMOS differential pair and NMOS cascode load. Due to the usage of PMOS transistors at the input terminals, the input voltage can come close to the negative rail. NMOS differential input pairs, unlike PMOS differential input pairs, operate near the positive supply rail. By combining the combination of both configurations, a parallel-connected PMOS and NMOS differential stage reaches operational mode at both rails. The rail-to-rail output stage reduces voltage drops at the output branch so that the output can reach the rails. The output stage is configured with a common-source NMOS and PMOS connected at the drain. The operating point is one of the most important factors to consider when designing the push-pull inverter output stage. The voltage input of this stage is the output voltage from the preceding stage. Two transistors in the push-pull inverter output stage are in the saturation region at this voltage. The current is largely dependent on the size of the transistors because there is no current bias network.

2 Implemented Circuit

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

[1] M. A. G. Lorenzo. Design and implementation of cmos rail-to-rail operational amplifiers. https://ieeexplore.ieee.org/document/4391985.