Design and Analysis of TSPC D flip-flop using eSim

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Abstract

This paper presents the design and simulation of a true single phase clocked {TSPC} D flip flop. D flip flops are the most widely used storage elements, it senses the D input at a particular edge of the clock {rising or falling edge} and delivers the output without getting affected by other parts of the clock. Since its proposal, true single phase clocked logic has widespread applications in the digital domain because of its less power consumption and less area occupancy than other methods. In this paper, the simulation and analysis of the TSPC D flip-flop is done on the eSIM software and compared with the reference simulation results of the same circuit to verify the results.

1 Circuit Details

As the design is a positive edge triggered TSPC flip flop, we will observe the output changing over the positive edge of the clock. When the clock signal Clk = 0, the first input inverter is in On state and the inverted D input reaches node A. The second {dynamic} inverter is in the precharge mode as M6 is in Off state and node B is charged up to Vdd {high}. As we see, during this low phase M8 and M9 are also off, therefore the last inverter holds its value and the output is stable during the low phase of the clock. During the high phase, the input inverter is off so the previous inverted D input is stored on A. Second inverter evaluates since M6 is on this time i.e. if A is high {1}, B discharges and if A is low {0}, then B remains high because in that case both M4 and M5 will be off, also M9 is on. So, the D-input loaded during the falling pulse reaches output Q and is maintained till another rising edge is encountered. When Clk makes a Low-to-High transition, the Qb will latch the complement of the input and Q will pass the input to the output. Also, if the preset input {Reset} is low the preset PMOS will be On and Qbar maintains its value High as long as Reset is Low. The simulation results will be checked on the eSIM software and the different waveforms that will be analyzed will be Clk, Reset, D input, and Q output.

2 Implemented Circuit

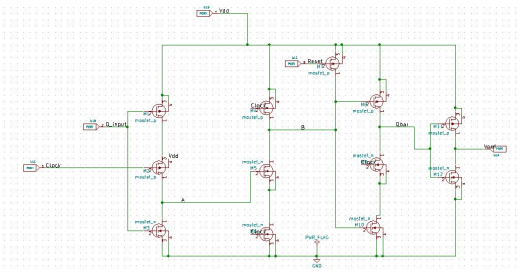

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

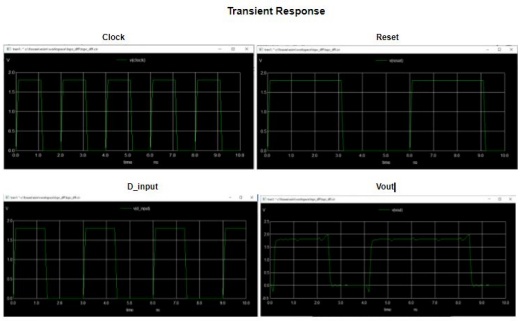

Figure 2: Implemented waveform.

References

[1] J. Shaikh and H. Rahaman. High speed and low power preset-able modified tspc d flip-flop design and performance comparison with tspc d flip-flop. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8379677.