CMOS Inverter

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Abstract

The input voltage can be complemented by using a simple NOT gate which can be considered as a basic inverter circuit that can be obtained by using two opposite-polarity MOSFET in a complementary manner. The CMOS inverters are the most widely used circuits in chip design that are used to invert or compliment the input signal. Hence by performing a simulation of the given circuit it gives us a short description of input and output characteristics, MOSFET states at different input voltages, and power losses due to electrical current. The CMOS inverter is an important circuit that provides a quick transition time and low power dissipation. As the result, this inverter has become more popular.

1 Circuit Details

A CMOS inverter consists of two MOSFET's that are PMOS and NMOS transistors that are connected at the drain and gate terminals. A supply voltage Vdd of 5V is applied at the PMOS source terminal and ground is connected at the NMOS source terminal. The input voltage Vin of 0 - 5 volt pulse is connected to the gate terminals junction of both the transistor and the output voltage that is Vout is connected to the drain terminal junction of both the transistor as shown in the circuit diagram. As the voltage at the input varies from 0 and 5 volts, the state of operation of the NMOS and PMOS varies accordingly, and hence the output voltage obtained is the inversion of input voltage. The working of two transistors that is PMOS and NMOS is as follows: When the applied input Voltage that is Vin is at a low state, transistor NMOS doesn't conduct whereas transistor PMOS conducts and stays in ON state because, as we all know the working of PChannel MOSFET and N-Channel MOSFET where NMOS transistor conducts only when the gate voltage applied is high or at a logic high state and the PMOS transistor conducts when the gate voltage applied is low or at a logic low state. Similarly, when the applied input Voltage that is Vin, is at a high state, transistor PMOS doesn't conduct whereas transistor NMOS conducts and stays in the ON state. As a result, we get an inverted waveform at the output.

2 Implemented Circuit

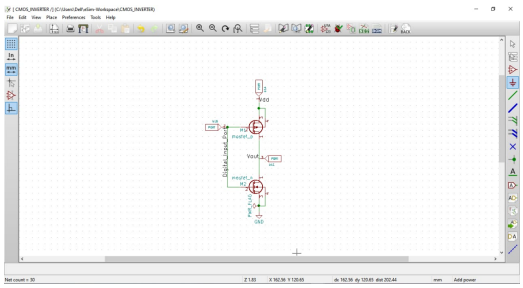

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

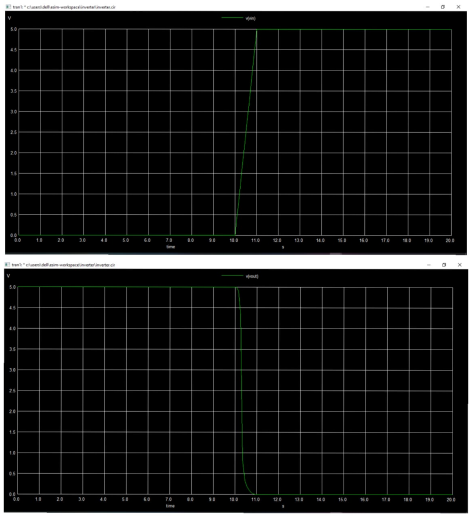

Figure 2: Implemented waveform.

References

[1] N. S. Dayanasari Abdul Hadi and S. W. M. Hatta. Reliability study of 90nm cmos inverter. https://ieeexplore.ieee.org/document/5700968.

[2] J. P. Uyemura. The cmos inverter. https://link.springer.com/chapter/10.1007/978-1-4615-3620-8_3.