Two Input NOR gate using CMOS

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Abstract

In this report design of two input NOR gate using CMOS is presented. NOR gate is one of the universal gate and can be used to design other gates and complicated circuits. It gives HIGH output only if both the inputs are LOW for all the other combinations of inputs it gives LOW output. This gate is implemented using CMOS circuit which consists of both NMOS and PMOS. We can easily implement circuit of basic gates using CMOS. Here the circuit is simulated using esim and ngspice and sky130 is used for the components i.e. PMOS and NMOS. Circuit diagram and waveform showing the trans analysis is presented below.

1 Circuit Details

In the given CMOS NOR gate circuits two PMOS i.e. M1 and M2 and two NMOS i.e. M3 and M4 are used. Inputs are given at vin1 and vin2 and output is obtained at vout. Input from vin1 is given to M1 and M4 and input from vin2 is given to M2 and M3. Source terminal of M1 is connected to the positive voltage vdd and drain is connected to the source of M2 i.e M1 and M2 are in series , drain of M2 is given to vout. Source of both M3 and M4 are grounded and their drain terminal are connected together to the vout, i.e. M3 and M4 are parallel. PMOS is ON if the input is LOW and OFF if the input is HIGH , NMOS is ON if the input is HIGH and OFF when input is LOW. The output at c will be HIGH only if both M1 and M2 are ON and M3 and M4 are OFF. Here vin1 is given a digital pulse with HIGH voltage of 1.8V and LOW of 0V and input is HIGH at 0us, 10us, 20us and so on for the interval of 5us. vin2 is given a digital pulse with HIGH voltage of 1.8V and LOW of 0V and input is HIGH at 0us, 20us, 40us and so on for the interval of 10us. vdd is given 1.8V and output at vout is HIGH i.e. 1.8V at 15us, 35us and so on for the interval of 5us, this is the time interval when both vin1 and vin2 are 0V, for all the other time interval vout is LOW i.e. 0V. Since the output is high only when both the inputs are low, it is working as a NOR gate.

2 Implemented Circuit

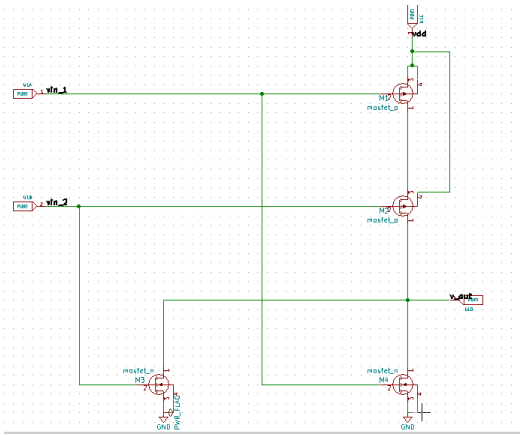

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

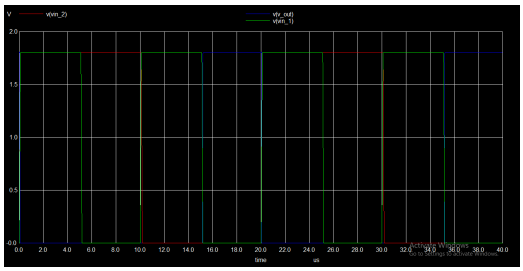

Figure 2: Implemented waveform.

References

[1] B. A. Rawi. Exciting stuck open faults in cmos circuits using ilp techniques. https//ieeexplore.ieee.org/abstract/document/1618388.