

Low Voltage CMOS Schmitt Trigger

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Abstract

Schmitt triggers are extensively used in digital as well as analog systems to filter out any noise present in a signal line and produce a clean digital signal. It is a comparator circuit that incorporates positive feedback with a hysteresis shaped transfer characteristic. The approach is based on studying the transient from one stable state to another when the trigger is in linear operation. However, this circuit will exhibit racing phenomena after the transition starts. Low Voltage CMOS Schmitt Trigger circuit is capable of operating in low voltage 0.8V to 1.5V at high capacitance, less propagation delay and stable hysteresis width. Low Voltage CMOS Schmitt Trigger is designed using SkyWater Open Source PDK and eSim.

2 Implemented Circuit

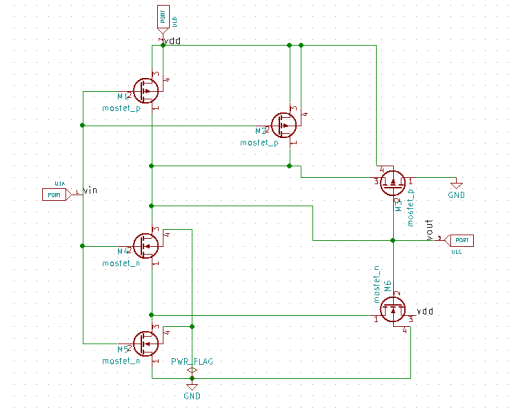


Figure 1: Implemented circuit diagram.

1 Circuit Details

CMOS Schmitt Trigger has two possible states trigger for circuit to change states is the input voltage level and changes only as input crosses a predefined threshold . Standard Schmitt Trigger is formed by a combination two sub circuit P and N sub circuit containing PMOS and NMOS respectively . Power consumption of CMOS consists of dynamic and static components . Since P sub circuit is connected to the path between the source voltage and output while the N sub circuit is connected between the path of output and ground. Therefore no static power consumption due to no direct path between source voltage and ground. In Low voltage Schmitt trigger circuit Part 1 of the designed circuit forms a NAND gate. Two PMOS M1 and M2 by a parallel and two NMOS M4 and M5 are formed by a series connections. Designing the PMOS in parallel the resistance of the P sub circuit is reduced by halves thus propagation delay can be reduced . Part 2 of the designed Schmitt Trigger consists of a PMOS M3 and NMOS M6 where both the MOSFET is directly connected through the gate terminal of each. The M3 act as pull up while M6 act as a pull down for the output at each case. By increasing width of PMOS it moves the switching threshold voltage towards vdd which makes hysteresis width more rectangular . When input vin is low only the P sub circuit will be considered and causes output to be high where both M1 and M2 are on but M3 is off hence the output voltage is pull to vdd . When input increases to vdd M4 and M5 is turned on while M6 is off. Output voltage is pull down to GND . It is taken across vout .

3 Implemented Waveforms

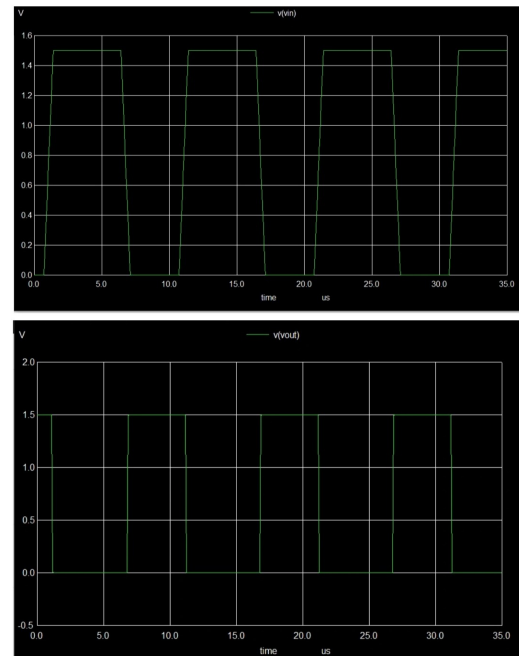


Figure 2: Implemented waveform.

References

- [1] M. Z. S. A. M. C. Faiz Arith, M. Idzdiar. Idris. Low voltage cmos schmitt trigger in 0.18 μ m technology.

core.ac.uk/download/pdf/235646717.pdf,IOSR Journal of Engineering (IOSRJEN),Vol. 3 Issue 3 March 2013.

- [2] H. B. I.M. Filanovsky. Cmos schmitt trigger design. <https://ieeexplore.ieee.org/document/260219>.
- [3] T. Y. M. M. H. Pranay Kumar Rahi, Shashi Dewangan. Design and simulation of cmos schmitt trigger. IJSET International Journal of Innovative Science, Engineering and Technology Vol. 3 Issue 8 August 2016.