The Two Stage CMOS Operational Amplifier with Frequency Compensation

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Abstract

This Paper proposes the implementation of Operational Amplifier based on CMOS Technology. It operates with single supply with voltage range from 3V to 5V. This Two stage OPAMP design includes Biasing Circuit, first stage of Differential amplifier with current mirror load, compensation circuitry and second stage of gain which is common source amplifier with active load. Simulation results of reference circuit gives the unity gain bandwidth of 4 MHz, Voltage gain of 65 dB with 65 deg phase Margin. Proposed OPAMP circuit design proves to be efficient as it operates at very low power i.e. in uwatts. This reference circuit will be simulated in eSim EDA tool and then will be implemented using SkyWater's 130nm PDK.

1 Circuit Details

OPAMP i.e Operational Amplifier is a basic building block of most of the Analog and Mixed Signal Design. Typically design of OPAMP is application specific so it has to be optimised to get the various specifications such as High gain, High Bandwidth, High CMRR and Large output swing etc. The Two Stage CMOS OP-AMP design can be divided into four parts. First part is Biasing Circuit which consists of transistors Mb1 to Mb6. It provides the reference current of 20uA to OPAMP with low Rout and low PVT sensitivity. Second Part of Design is Input Differential Amplifier stage. Here Differential input voltages are applied to transistors MP1 and MP2 forms. These transistors will convert these voltages into proportional differential currents which are then applied to current mirroring transistors MN1 and MN2. Output of this stage is taken at Drain of MN2. Required bias current to all transistors MP1 MP2 MN1 MN2 is given by MP3 by current mirroring action. Third Part of Circuit is RC compensation circuit. Output current from MN2 is passed through series combination of Rc and Cc. Here Cc i.e. Compensating Capacitor is used to provide frequency Compensation. This improves the Phase margin to get the stability. The Series resistor Rc transforms the RHP Zero to the LHP which provides additional Phase lead and hence improves the Phase Margin. Fourth Part is the last stage of OPAMP which is simple CS amplifier stage consists of MN3 as CS transistor with MP4 as current source load. Finally the output of OPAMP is taken at drain of MN3 and MP4.

2 Implemented Circuit

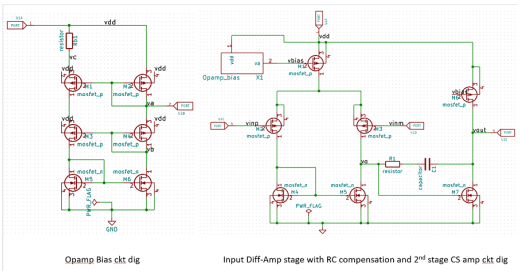

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

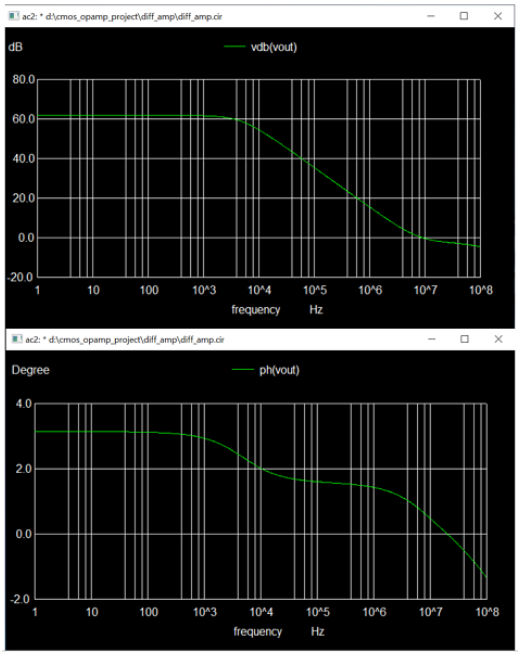

Figure 2: Implemented waveform.

References

[1] A. Sedra and K. Smith. Reference book - microelectronic circuits theory and application. https://easyengineering.net/microelectronic-circuits-theory-and-application.

[2] A. Yodtean and C. Punyasai. A design of cmos operational amplifier in tmec 0.8 um technology. https://ieeexplore.ieee.org/document/8620012.