Implementation of Full Adder using SkyWater 130nm PDK

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Abstract

The logic gates are the fundamental building block of digital system like adder, comparator, etc. This paper proposes implementation of a full adder using XOR gate. So, in this paper Full Adder circuit is made by using CMOS technology and implement it. Full Adder circuit is implemented by using ten transistors along with the three 1-bit full adder cells. From the simulation process it was found that this has better performance in terms of power consumptions, delay and power delay product. It was observed that, the circuit has achieved maximum power saving of 91.54 percent, saving delay of 59.7 percent and overall saving of 91.65 percent. This circuit operates with 1V power supply.

1 Circuit Details

Till today, different types of full adder cell are made and designed with different logic styles in digital world. In that some of them are good low power consumption, some of them for high speed and few for minimum area requirement but all these circuits have its own merits and demerits. According to the required application these full adders are used. Few of the full adder cells which are already implemented are convectional full adder, Static Energy Recovery Full Adder cell, Gate Diffusion Input full adder cell, etc. For most of the complex computational circuit requires full adder are used. Due to this, the whole power consumption and speed of computational circuit can be managed by the implementing the low power and high speed adder cell. So performance is totally depends on full adder. A full adder cell consists of three inputs and two outputs. Some of them are Expression for sum and carry out Sum = A'.b'.Cin +A'.B.Cin'+ A.B'.Cin'+ A.B.Cin = (A xor B) xor Cin Carry out (Cout) = A'.b.Cin +A.B'.Cin+ A.B.Cin' +A.B.Cin = A.B + B.Cin + Cin.A = (A xor B) Cin + (A xor B)' B This circuit is implemented with help of ten transistors. This circuit was implemented by using XOR gate. It uses two XOR module section and one inverter section. Each XOR module section is made by using 2 PMOS and 2 NMOS transistors. This is done which gives a better power and delay when compared to other circuits of full adder.

2 Implemented Circuit
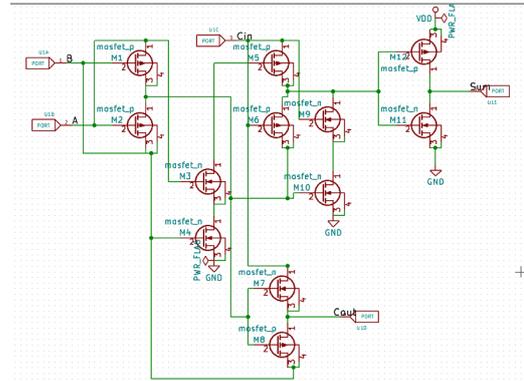
Figure 1: Implemented circuit diagram.

3 Implemented Waveforms
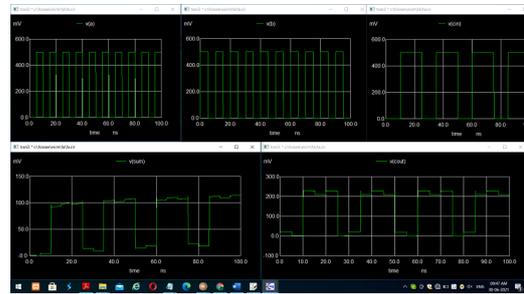
Figure 2: Implemented waveform.

References

[1] A. K. D. Ashish Kumar Yadav, Bhavana P. Shrivatava. Low power high speed 1-bit full adder circuit design at 45nm cmos technology. https://ieeexplore.ieee.org/document/8378203.