2:4 Decoder using mixed logic CMOS gates

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Abstract

This paper introduces the design of a low power 2:4 decoder using 14 CMOS transistors. Decoder is a combinational circuit and is widely used in the periphery circuitry of memory arrays like Static RAM. The circuit is designed using a mixed logic style which is a combination of Transmission Gate Logic (TGL) and Dual Value Logic (DVL). The circuits that are designed using mixed logic exhibit better performance and more compact when compared to the circuits designed using the static CMOS logic. The proposed circuit will be implemented in eSim EDA and the simulation will be done using the Sky 's 130nm PDK.

1 Circuit Details

A 2:4 line decoder has two inputs, A and B where A is the MS bit and B is the LS bit. It has four minterm outputs, D0 = A'B', D1 = A'B, D2 = AB' and D3 = AB. It can be designed by using TGL or DVL gates as it takes 16 transistors which includes 12 AND/OR gates and 2 inverters. By using some proper signal arrangement, we can eliminate one of the two inverters A or B; Here D0 and D2 is implemented by using DVL logic, while D1 and D3 is be implemented by using TGL logic. For D0 and D2, A is the propagate signal, and for D1 and D3, B is the propagate signal; this eliminates the inverter B. Hence, the 14-transistor decoder consists of 9 NMOS and 5 PMOS for the low power decoder. The same low power 2:4 decoder can also be realised if we interchange the position of the TGL and DVL of the minterms in the above configuration. This is called inverting topology. Here also the elimination of inverter B is done. Thus, there is overall reduction of two transistors, logical effort, switching activity and also power dissipation in both the topologies. The topologies can be termed as 2:4 LP and 2:4 LPI, I for invert. In our circuit, the 2:4 LP decoder will be implemented and simulated. The necessary circuit diagrams are attached.

2 Implemented Circuit

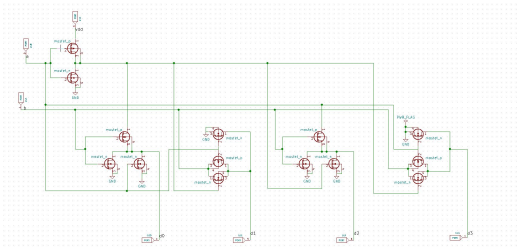

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

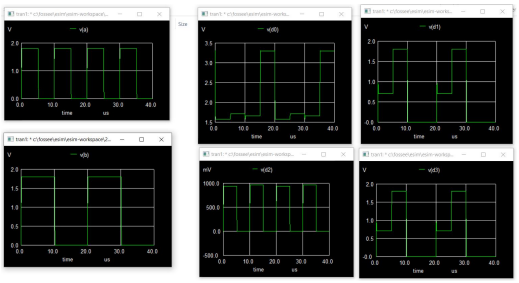

Figure 2: Implemented waveform.

References

[1] P. P. K. Medapati. Low-power and high-speed 2-4 and 4-16 decoders using modified gate diffusion input (m-gdi) technique. https://www.researchgate.net/publication/342422147.