

Darlington amplifier

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Abstract

In today's communication system, the demand of transistors is very high having high data rate. The main thing that attracted me is that is a multi-transistor configuration called the Darlington configuration commonly called a Darlington pair. Darlington transistor is one that offers a high current gain and also give back high input impedance. This configuration has a much higher current gain than each transistor taken separately. It acts like a single transistor. A Darlington transistor acts as a single transistor with high current gain, it means that a small amount of current is taken from a microcontroller. Transistors are used in many applications where high gain is needed by using very low frequency.

1 Circuit Details

In the present paper, we proposed various modifications in small signal pair amplifier circuit and calculated some different results that may be useful for various applications. In comparison to bipolar conventional pair, we can also design a MOSFET configuration to reduce supply voltage (VDD) and dc consumption power. If we increase the collector current in pair amplifier, DC consumption power also increases and noise also increases, we can remove this disadvantage by designing a single input single output (SISO) amplifier based on MOSFET pair configuration. In this design NMOS and PMOS is used wherein here the output of NMOS is given as the input for PMOS that is CMOS. Some resistances and capacitors are used with different values. One capacitor is used as load capacitor and another one input capacitor is also on this circuit. In electronics, amplifying signal by using pair is very important. The value of resistances used are 22k Ω , 5k Ω , two 100 Ω , two 1k Ω . Two capacitors are used in the proposed circuit one at the input terminal and one at the output terminal as a load, and the value of capacitors used are 22 μ and 1 μ . Recently Darlington cell and Darlington topology have been reported high gain and good bandwidth for modern application. In transient response time is varying with voltage and current. Other parameters and DC biasing supply that are used to design respective circuits. The performance of pair amplifier is very poor at high frequency and then the output will be verified.

2 Implemented Circuit

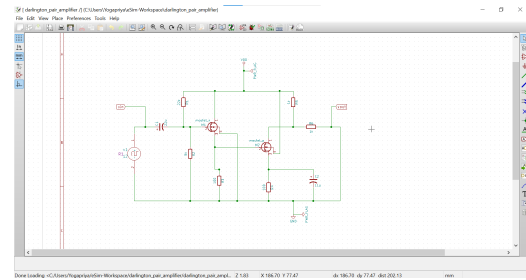


Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

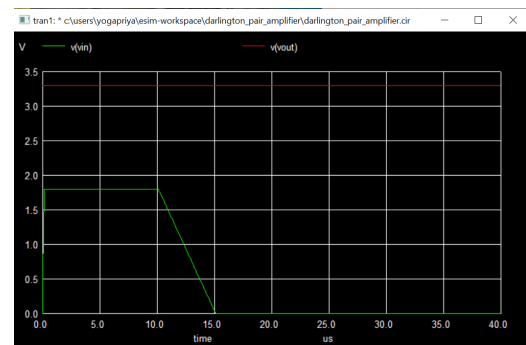


Figure 2: Implemented waveform.

References

- [1] E. R. s. Dr. Rajesh Mehra. Analysis of darlington pair amplifier at 90nm technology. <https://ieeexplore.ieee.org/document/7755385>.