Low Power CMOS Analog Multiplier using skywater 130nm pdk

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Abstract

Analog Multiplier is a circuit mainly used for analog signal processing applications. The output of the circuit is product of two or more independent input voltages. So the size and working of the circuit should be designed carefully to consume less power which results in increased battery life. The aim of the design is to make a multiplier circuit that consumes less current and able to run on low voltage input power supply. The analog multiplier circuit has been designed using sky 130nm Complementary Metal Oxide Semiconductor technology. The circuit can be operated using 1.2v voltage supply and the power consumption is less.

1 Circuit Details

The analog multiplier is used to multiply two continuous input signals, say v1 and v2 and produces output as v which is the linear product of two inputs. The output can be expressed as v=k v1 v2, where k is the gain. The circuit design proposed in this paper is used to eliminate extra voltage reference to provide a compact circuit design. By using CMOS technology with 130nm, the device density and performance can be improved. Low power consumption can be also achieved using the same technology. The circuit consists of a pair of common source amplifier with input transistors m9 and m10. The output is the squared function of input voltages v1 and v2. The circuit is built using 8 PMOSs and 2 NMOSs with two resistors. Transistors of m1 to m8 are of the type PMOS and transistors of m9 and m10 are of the type NMOS. The resistor value is taken as 2.5kOhm to make all the transistors present in the circuit to work in proper region. Transistors m1 to m8 acts as square root circuit in non-linear cancellation path. The output current from the input transistors m9 and m10 are directed into the square root circuit block which results in producing differential output voltage or current which is the multiplication of the input signals v12 and v34. v12 signal is the difference between v1 and v2 input signal, whereas v34 signal is the difference between v3 and v4 input signal. The resulting output signal v is the differential output of vout1 and vout2. The circuit can be able to operate with an input voltage of 1 to 1.2v and the measured power consumption is between 35uW to 98uW.

2 Implemented Circuit

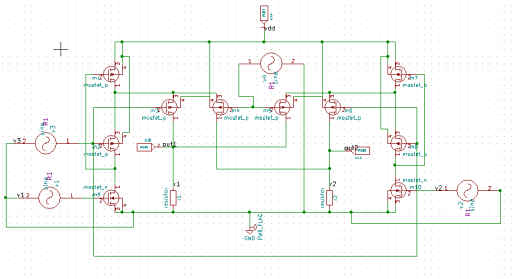

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

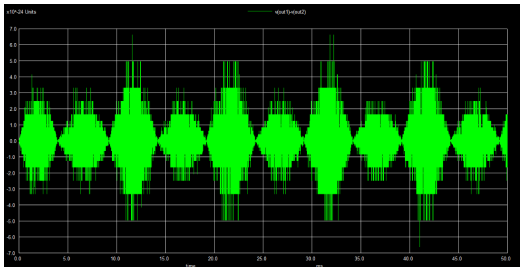

Figure 2: Implemented waveform.

References

[1] A. S. A. Naim and S. H. Ruslan. 130nm low power cmos analog multiplier. https://www.researchgate.net/publication/326510092_130_nm_Low_