Design of Half Adder using CMOS Technology

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Abstract

The important components in digital design are Half adders. They perform many arithmetic operations. CMOS stands for Complementary Metal Oxide Semiconductor. It is used for manufacturing integrated circuits. Studies performed have shown that circuits using CMOS technology are more efficient realizations and have a wider range of different logic cells and are used for realistic circuit arrangements. CMOS is superior to CPL in most cases with respect to speed, dissipation, power, area and power-delay products. Half Adder designed using CMOS technology have more power as well as speed. The paper describes Half adder described using CMOS technology and proves that it is an efficient method.

1 Circuit Details

Half adder is a combinational circuit that performs simple addition of two single bit binary numbers and produces a 2-bit number. The LSB of the result is the sum and the MSB is the Carry. In the basic approach the half adder is implemented using the primitive logic gates i.e., XOR and AND for sum and carry respectively. Here in the project Half adder is implemented using the principle of the static (CMOS) technology. This helps us in making the size of fabrication more small in terms of nanometre and hence making it compact yet efficient. The (CMOS) comprises of (NMOS) and (PMOS). There are two inputs and two outputs in a Half Adder. Inputs are named as A and B, and the outputs are named as Sum (S) and Carry (C). The appropriate sum and carry logic is realised and the circuit is represented using pull up and pull down transistors i.e. pmos and nmos transistors for the logic. The circuit for sum and carry are separately implemented in the same schematic. Required Inputs are inverted using pmos and nmos inverter design .Here in the circuit the inputs A and B are inverted using the inverter circuit , Ab and Bb are the other two inputs obtained using these respective logic are generated for sum and carry. Required ground and power supply is provided in the circuit. The circuit is annotated and the Netlist is generated using eSim. The python plot for sum and carry are obtained along with ngspice inputs A, B.

2 Implemented Circuit

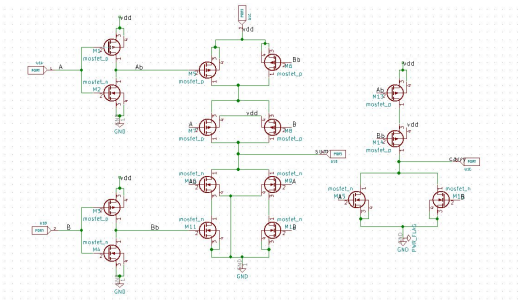

Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

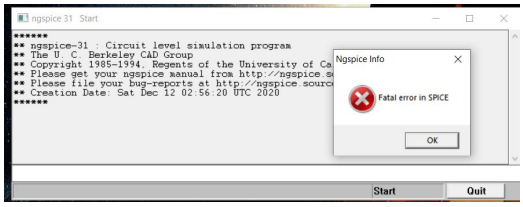

Figure 2: Implemented waveform.

References

[1] G. D. R. G. B. G.Hemanth Kumar, N.Harish. Design of low power half adder using static 125nm cmos technology. https://www.researchgate.net/publication/330086278_Design_of_Low