# Logic NAND gate design using Cmos

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July 1, 2021

## Abstract

In this paper you can see the design of basic NAND gate using CMOS technology. Here I have used 2 NMOSFETs 2 PMOSFETs voltage sources and one capacitor. Both the pmos are connected in parallel and their shorted drain terminal is connected to the nmos drain. And both nmos are connected in series. I am taking all the mosfets of same width and length to get the good waveforms. This circuit schematic is drawn in eSim EDA free software tool. And waveforms are observed in the simulation window of eSim tool. For designing this circuit I have referred the below mentioned resource paper. We can even connect a capacitor of smaller value at the output terminal for better waveform observations.
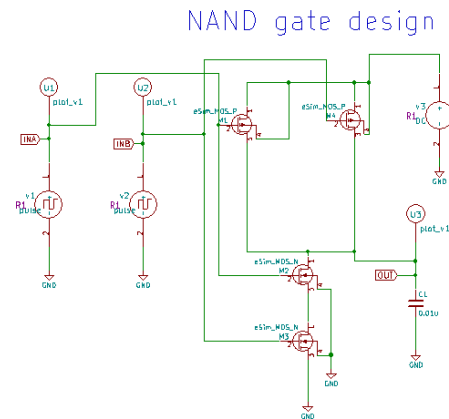
## 1 Circuit Details

For NAND gate design we are connecting 2 pmos in parallel and 2 nmos in series and pulse voltages of different pulse widths and different periods are connected to the gate terminals of both pmos and nmos to observe all possible outputs. Then I connected a DC voltage source to the source and bulk terminals of both pmos, and bulk of Nmos to the Vss or ground terminal . I am taking all the mosfets of same width and length we can call it as aspect ratio. I taken aspect ratio as 20/5 to get the good waveforms. I kept both width and length in micro meters. And input DC voltage source is 5V. We can very the DC input but minimum input should be greater than the threshold voltage of the mosfets. for my requirement I made sure that all the mosfets are in saturation region. because in saturation region we can observe a linear relation ship between input and output voltage. And one more condition to keep in mind is we should not keep the mosfets in cutoff region. Because in cutoff region mosfet will not allow the current to pass through it. We can say that mosfets will be off in cutoff region. This circuit schematic is drawn in eSim EDA free software tool. And waveforms are observed in the simulation window of eSim tool. We can connect a capacitor of smaller value at the output terminal for better waveform observations. As we already know that NAND gives the inverted outputs of AND gate. Hence for the NAND gate out outputs will be 1 1 0, 0 1 1, 1 0 1, 0 0 1. Here first two bits shows two inputs and last bit is the output.

## 2 Implemented Circuit



Figure 1: Implemented circuit diagram.
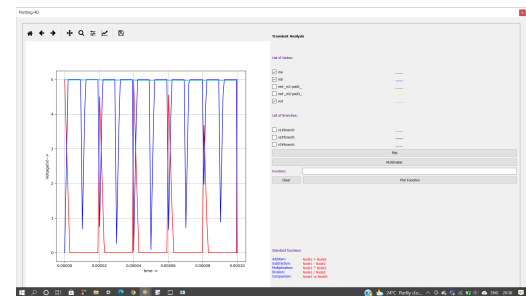
## 3 Implemented Waveforms



Figure 2: Implemented waveform.

## References

[1] M. Annaratone. Designing combinational logic gates in cmos. bwrcs.eecs.berkeley.edu/Classes/icdesign/ee141f01/Notes/chapter6.p