8T FULL ADDER

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Abstract

The project is to implement 8T full adder using esim and done using SKYWATER's 130nm PDK. Adders are the main components to perform many important arithmetic operations like multiplication, addition, division, and many other. Hence, full adder becomes the most required component for many digital circuits. In most of these digital circuits, adder lies in the critical path that affects the overall speed of the system. To improvise the performance of the 1-bit full adder is the main task. So, an 8-transistor full adder (8T full adder) is used which shows the discharging problem at the carry output for some combinations. This circuit challenges to overcome the disadvantage created by the existing 8T FA.

1 Circuit Details

This circuit 8T full adder is designed using 3 XOR gates. Here,8 MOS transistors are used to create this circuit in which 5 transistors are PMOS transistors and 3 are NMOS transistors. This circuit is a proposed version of existing full adder as it helps in overcoming in discharging at carry output for some combinations of input. In the existing version of the circuit, they used 4 PMOS transistors and 4NMOS transistors in which the combination of 2 NMOS transistors (M7, M8) produces carry where the discharge is happening. When the input A=1, B=0 and Cin=1 is applied to the existing model, it should produce sum as logic '0' and carry as logic '1', but it produces carry as logic '0' because the M8 NMOS transistor switches ON along with M7 NMOS transistor creating ground path for the carry. And, when input combinations of A=0 and B=0 are applied, it is producing an undefined output at the carry. Here, in the proposed circuit, M7 transistor is PMOS which helps in overcoming the disadvantage by feeding transistor M7 with the 'A xor B' signal that enables only one transistor in the carry part such that the discharging part can never be created for all the combinations of input. Here, 3 inputs A, B and Cin are given, and outputs Sum, and Carry are taken from the circuit. The full adder is implemented using Boolean expression for sum and carry as: Sum=A xor B xor Cin Carry=AB+BCin+CinA= AB+Cin(A xor B)
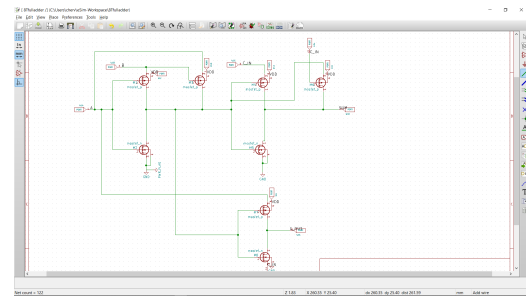
2 Implemented Circuit

Figure 1: Implemented circuit diagram.
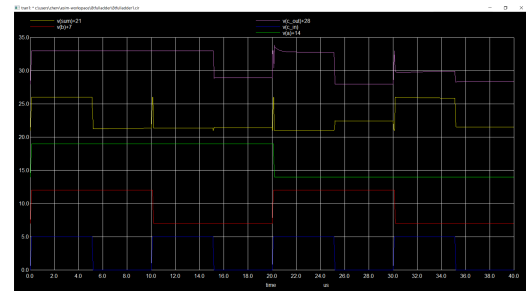
3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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