D Flip Flop using CMOS Technology

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Abstract

The circuit implementation of D flip flop using CMOS technology has been inspired from the one earlier implemented with 90nm technology. D flip flop plays an important role laying foundation stones to building an efficient modern digital circuit. This paper consists the implementation of D flip flop with PMOS and NMOS transistors using multi threshold CMOS technique. Results reflect that MTCMOS technique which is employed improves speed of circuit and reduces leakage power effectively. High speed and low power consuming IC can be achieved by reducing transistors geometrical size. The proposed circuit will be implemented in eSim EDA tool and done using Sky Water 130nm PDK.

1 Circuit Details

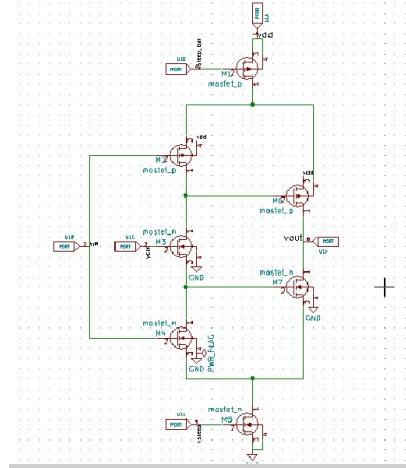D Flip Flop is a bistable circuit which gives two outputs either 1 or 0 depending on the input and clock pulse. D in D flip flop stands for Delay or Data meaning the flip flop reciprocates the output as found in the input. D flip flop is edge triggered so when clock pulse is applied and value of D in the input is 1 the flip flop undergoes SET state and output Q is 1 similarly if the value of D is 0 the flip flop undergoes RESET state therefore the output becomes 0. D flip flop is used for various applications like data synchronizer frequency divider event detectors and to create delay lines. The circuit shown in the figure is implemented using multi threshold complementary metal oxide semiconductor MTCMOS it consists of 3 PMOS transistors and 4 NMOS transistors. There are various inputs for this circuit namely 1. data input vin which takes input voltage from the input port 2. vclk which represents the clock signal 3. vsleep and vsleep bar are two separate port whose signals are used to reduce power dissipation . The output of the flip flop is shown in the vout port . The voltage range for vin and vclk is varied from 0 to 1.8V at steps of 5us and 4us respectively vdd is varied from 0 to 3.3V vsleep and vsleep bar is varied from 0 to 2.5V to get the D flip flop waveform As seen in the waveform vout changes only during the positive edge of the clock pulse and hence this circuit is a single edge trigger flip flop. NOTE when the clock pulse is not applied the output of the flip flop does not change and is in high impedance state.

2 Implemented Circuit

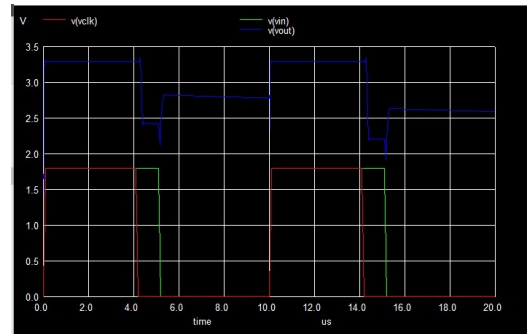Figure 1: Implemented circuit diagram.

3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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[2] H. Chao and C. Johnston. Behavior analysis of cmos d flip flops. https://ieeexplore.ieee.org/document/572637.

[3] S. Rahman and T. Chandel. Schematic design and layout of flipflop using cmos technology. https://www.researchgate.net/publication/320065130_Schematic_Des